UNIFIED ACCURATE CAD MODELS FOR RF, MICROWAVE AND MILLIMETER-WAVE INTEGRATED CIRCUITS

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Abstract - **Unified CAD-oriented circuit model is proposed and developed for accurate representation of a variety of planar integrated circuits (ICs). It is realized by implementing a so- called "short-open calibration" (SOC) procedure that uniquely calibrates (de-embeds) the results obtained from a full-wave method of moments (MoM) with two calibration standards: short and open elements. Stemming from the concept of TRL calibration in the microwave measurements, this SOC is used to evaluate and to remove unwanted numerical error terms. These error terms mainly come from the approximation of excitation mechanisms in the deterministic 3-D MoM and inconsistency between the 2-D and 3-D MoM-based simulations of uniform line sections. Following a brief description of our modeling technique related to the SOC and 3-D MoM, different classes of planar structures are characterized in terms of their CAD circuit models that involve all physical effects, such as frequency dispersion, high-order mode effects and unbounded radiation losses. The circuit models developed herewith are very useful not only in gaining physical insight into the electrical behavior of planar structures and also in implementing efficient circuit network-oriented design/optimization approaches. The SOC-extracted circuit parameters are presented for microstrip interdigital capacitor (IDC) and finite-ground CPW gap structures, which are also well verified by our measurements.**

I. INTRODUCTION

With the rapid development of RF, microwave and millimeter-wave ICs, significant interests have been aroused towards exploring a joint field/circuit scheme for accurate modeling of planar circuit elements, which allows an efficient design of planar circuits or systems as a whole with field-theory-based results and circuit-network-based tools. In the last decades, the full-wave method of moments (MoM) [1−9] has widely been studied and used as one of the most powerful modeling techniques for field-based characterization of shielded and unbounded planar circuit structures, in the form of a dielectric layer and/or multi-port. The MoM algorithms have generated several high-profile commercial EM simulator packages [10], which are very useful for the simulation of planar circuits and antennas.

Also, a significant amount of peripheral works in this connection has also been done and they were essentially oriented towards a field theory-based optimization procedure [11] in conjunction with EM simulators. Such a direct EM optimization tool requires, however, computationally intensive labor, and of course, an excessive CPU time and a huge memory space. In practice, the circuit designer always prefers the use of an optimization procedure based on well- established efficient and analytical network synthesis/optimization tools [12]. Therefore, the key issue is how to self-consistently formulate or to extract the CAD- oriented equivalent circuit models of a planar structure from field-theory calculations. This is critically important to bridge the gap between the two aspects: field-based simulation analysis and circuit-based optimization design.

In our opinion, the MoM framework developed to date can essentially be classified into indirect and direct algorithms. The direct MoM algorithm has several attractive features such as its ability in the explicit formulation of multiport planar circuits or discontinuities in terms of the calculated electrical parameters at each port plane without resort to additional calculations. In [13], a deterministic MoM algorithm was developed for a full-wave modeling of unbounded planar microstrip circuits. It was done by simultaneously introducing impressed electric fields (voltages) at port planes. In this way, a source-type MoM matrix equation can be built up based on the Galerkin's technique.

Nevertheless, there is a common problem for all direct MoM algorithms that the impressed fields are theoretically impossible to simulate ideal dominant modes propagating along feed lines. Although this technique has been widely used for the full-wave simulation of usually electrically large planar circuits and antennas, very limited work has been reported to date for parametric extractions of basic and electrically small planar elements. Implicit error terms are responsible for such algorithmic handicaps, and they are mainly caused by the approximation of impressed fields [14], and also inconsistency of 2-D and 3-D MoM characterizations of uniform feeding lines in the de-embedding procedure [15].

Inspired from the concept of experimental calibration techniques such as Thru-Reflect-Line (TRL) [16], a numerical de-embedding technique, called "short-open calibration"(SOC), is developed to calibrate the MoM-calculated parameters. In this case, a planar structure of interest is in general classified into two distinct parts: error boxes (feed lines) and core circuit box (planar

discontinuity). Two standards of calibration, namely, short and open elements, are independently defined in the 3-D MoM for the de- embedding of circuit box parameters by evaluating and removing out the error terms related to each feed line. With the SOC scheme self-consistently formulated in the MoM, planar circuits can be characterized as their unified circuit models at selected planes of reference.

In this work, we will formulate CAD-oriented equivalent circuit models for a number of electrically small planar and uniplanar circuits, which are formed on the basis of microstrip, coplanar waveguide (CPW) and coplanar stripline (CPS). Through the use of our developed SOC procedure, their electric behaviors will be extensively investigated that exhibit their quasi-lumped-element and/or dynamic circuit performance over a wide range of frequency. Also, the proposed unified circuit model is very well verified by our measurements for some planar and uniplanar circuits reported in this work.

II. FULL-WAVE METHOD OF MOMENTS (MOM)

Fig. 1(a) and (b) describe the physical layout arranged for the deterministic MoM-based characterization of two classes of two-port unbounded microstrip (MS) and finite-ground coplanar waveguide (FGCPW) discontinuities, respectively. To formulate a source-type (direct) MoM algorithm, a pair of impressed field sources is simultaneously introduced at each port plane, #1 and #2, far away from the region of the core circuit discontinuity, as described in Fig. 1(a) and (b).

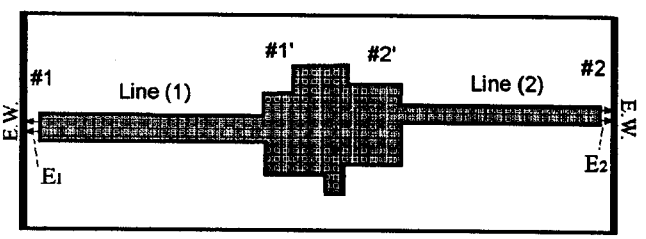
Due to different location of the signal strip and ground plane in the microstrip structure (Fig. 1(a)), an electric wall at each port is assumed to extend vertically the ground plane. As a result, the impressed fields can be longitudinally distributed at an infinitesimal interval between the electric wall and the end of the signal strip, as shown in Fig. 1(a). As for the FGCPW structure which finite-width ground and signal strip are both located at the same dielectric interface, the impressed fields can be explicitly introduced across the transversely infinite interval, as shown in Fig. 1(b), without requiring the assumption of electric walls at its ports.

As detailed in [13], our attention is focused on the intrinsic physical difference between the feed lines and circuit discontinuity. Only the dominant-mode wave can propagate along the feed lines while the circuit discontinuity is responsibility for all the discontinuity effects. In this way, the entire structure in Fig. 1(a) or (b) is divided into two separate parts: static feed lines and dynamic discontinuity, at reference planes of our choice, namely, #1' and #2'. Fig. 1(c) describes the equivalent circuit topology that consists of three networks, namely, error box [X_1] for the 1st line, core circuit network and error box [X_2] for the 2nd line. By applying the Pocklington's integral equation and imposing the field vanishing condition over the conductor surface, an electric field integral equation (EFIE) can then be established with the two distinct parts in mind, and it is expressed as,

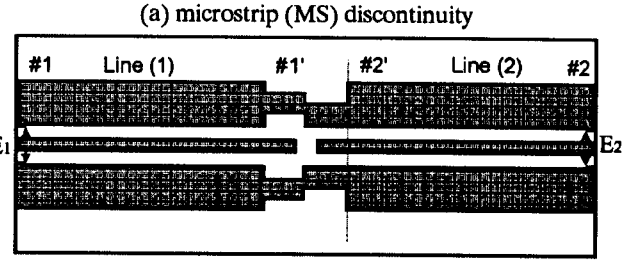
$$\sum_{i=1}^{2}\left[\vec{E}_i^{inc}(\vec{r}) + \iint_{line(i)} \mathbf{G}(\vec{r}/\vec{r}_s)\vec{J}_i(\vec{r}_s)\,dS_s\right] + \iint_{line(i)} \mathbf{G}(\vec{r}/\vec{r}_s)\vec{J}_i(\vec{r}_s)\,dS_s = 0 \quad (1)$$

in which G( ) denotes dyadic Greens function of the unbounded layered structure. $\vec{E}_i^{inc}(\vec{r})$ *(i=1,2)* are the impressed fields for i[th] line.

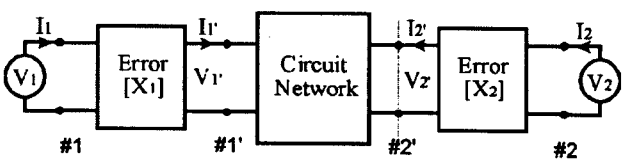
Next, the Galerkin's technique is applied to Equation (1) in formulating a spectral-domain integral equation in the form of a double integration. With the choice of the same number of the weighting functions as that of the basis functions, a source-type equation can then be formulated in a matrix form, as illustrated in [13]. Each impedance-type sub-matrix describes the interaction of two physical orientations. Moreover, two column sub-matrices, **(Vp)** and **(Ip)**, are associated with the impressed fields and current densities at each port of the feed lines. Thus, a deterministic MoM scheme has been built up for the quantitative field-based interrelation among all of the port voltages and currents.



(a) microstrip (MS) discontinuity



(b) finite-ground CPW (FGCPW) discontinuity



(c) unified equivalent circuit representation

Fig. 1: MoM-based physical layout of two classes unbounded MS and FGCPW discontinuities and their unified equivalent circuit representation.

III. SHORT-OPEN CALIBRATION (SOC) TECHNIQUE

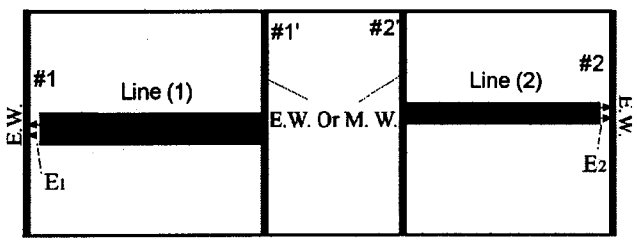
As described in Introduction, there exist error terms that jeopardize the de-embedding procedure of the true circuit model even though they may be very small. Now, a numerical calibration procedure is developed and applied for accurate parametric extraction of the unified circuit model at the reference planes, #1 and #2, from the MoM calculated results at the ports, #1' and #2'. In a similar manner to the concept of calibration procedure in the microwave measurements, the two error boxes, as defined in Fig. 1(c), allow one to deduce analytically equivalent voltages and currents at the reference planes of interest, V'_1, I'_1 and V'_2, I'_2 from those at the port planes, V_1, I_1 and V_2, I_2. These port voltages and currents can be obtained by the MoM calculations as in Section II.

Let's now define the two calibration standards in the MoM algorithm for accurate parametric evaluation of the error boxes. Fig. 2 illustrates the physical arrangement and network representation of the "short" and "open" elements at the reference planes of feed lines with reference to the two- port unbounded microstrip discontinuity of Fig. 1(a). The two feed lines are separately terminated with electric wall (E. W.) and magnetic wall (M. W.) for the formulation of microstrip short-end and open-end in the full-wave MoM scheme. As detailed in [17], a set of four equations can be derived for characterization of their related network topology in terms of an ABCD matrix. Consider the open-end case, the first equation is obtained with port voltage V_{i0} and current I_{i0} for i^{th} line

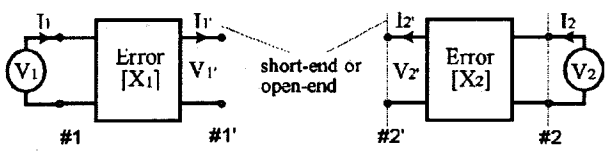
$$\mathbf{a_i} \cdot \mathbf{I_{iO}} + \mathbf{b_i} \cdot \mathbf{V_{iO}} = 0 \qquad (2)$$

Also, two other equations for the solution of ABCD matrix are established on the basis of network theory with the port voltage, the port current and the current flowing at the short- end,namely, ViS,IiS and I'iS, for the short-end case,

$$\mathbf{a_i} \cdot \mathbf{I_{iS}} + \mathbf{b_i} \cdot \mathbf{V_{iS}} = \mathbf{I'_{iS}} \qquad (3)$$



(a) physical arrangement for the SOC scheme



(b) equivalent circuit representation

Fig. 2: Physical arrangement and equivalent circuit representation of the SOC calibration standards: short and open elements, for the MS structure.

$$\mathbf{c_i} \cdot \mathbf{I_{iS}} + \mathbf{d_i} \cdot \mathbf{V_{iS}} = 0 \qquad (4)$$

Use of the transmission reciprocity of network leads to an additional equation, such as,

$$\mathbf{a_i} \cdot \mathbf{d_i} + \mathbf{b_i} \cdot \mathbf{c_i} = 1 \qquad (5)$$

To simplify our following description, all of the above equivalent currents are respectively normalized by the impressed port voltages, V_{iO} and V_{iS}, for the two proposed schemes of excitation. Through the solution of Equations (2- 5), the ABCD matrix of the i-th error box can explicitly be formulated by

$$[X_i] = \begin{vmatrix} I_{iS} / I'_{iS} & -1 / I'_{iS} \\ -I'_{iS}I'_{iO}/(I'_{iS}-I'_{iO}) & I'_{iS}I'_{iO}/(I'_{iS}-I'_{iO}) \end{vmatrix} \qquad (7)$$

This equation shows that the ABCD matrix of an error box can be accurately determined by three terms of numerically "measured" currents, I_{iO}, I_{iS} and I'_{iS}. These currents are flowing at the input port of the "open" element, the input port and the short-end of the "short" element, respectively, under the even- and odd-excitations of a pair of the unified impressed voltage sources. With this 3-D pre-calculated ABCD matrix, the equivalent voltage and current, V'_i and I'_i, defined over both sides of the circuit network that characterizes the planar discontinuity of Fig. 1, can be interrelated to the port voltages and currents, V_i and I_i. The numerical SOC technique is thus described to extract circuit parameters of the two-port unbounded microstrip discontinuity from our full-wave MoM scheme. This is the cornerstone in our proposed unified circuit model, and obviously it is easily extended to multi-port cases or other feeding line structures including hybrid topologies such as FGCPW-to-CPS transition structure.

IV. UNIFIED CAD CIRCUIT MODEL

In this section, the proposed SOC technique is used to handle a number of unbounded microstrip (MS), finite-ground coplanar waveguide (FGCPW) and coplanar stripline (CPS) circuits in terms of the equivalent circuit models based on the full-wave MoM algorithms. They are highly accurate field theory-based SPICE-compatible lossy circuit models, which involve all of the possible physical effects in a unbounded structure such as space-wave radiation, surface- wave leakage and high-order modes propagation as long as they are calculable with the MoM algorithm. Therefore, the developed unified model paves the way for the designer to apply directly field theory-based CAD techniques and optimization routines in the design and synthesis of microwave and millimeter-wave circuits and antennas.

To design an electrically large microstrip circuit, for example, it can be segmented into a number of basic electrically small circuit units in a dynamic manner. If required, a subsequent global optimization procedure or mapping technique can be applied to tune the circuit geometry that can be done in a very flexible way. As a matter of fact, the inter-element coupling can also be extracted to facilitate and minimize any potential tuning

procedure. This is one of the most attractive features of this new technique in contrast to other algorithms. In the following, our attention will be directed to characterize the circuit model of several basic unbounded structures. They are indispensable in the design and realization of a very large class of high-frequency integrated circuits and systems.

(A) MICROSTRIP INTERDIGITAL CAPACITOR (IDC)

A generalized microstrip interdigital capacitor (IDC) structure is studied for its coupling characteristics and dispersion effects. Fig. 3 describes its physical layout and equivalent circuit based on a J-inverter network representation. This J-inverter network that consists of a susceptance and two equivalent line lengths is transformed from the pre-calculated and extracted Y-matrix according to the equivalence of these two networks. The J-inverter susceptance, J, is proportional to the capacitive coupling of the IDC, while two attached electrical lengths, ϕ_1 and ϕ_2, represent the dispersive fringing fields and finger-end discontinuity effects in the IDC.

Fig. 4 plots a set of curves for the extracted J-inverter susceptance and two equivalent electrical lines as a function of frequency for a symmetrical IDC versus the number of finger ($N = 2, 4, 6, 8, 10$). In this example, the strip width is equal to the overall dimension of the multiple finger section, and only the finger ends then contribute to parasitic effects occurring around the finger section. It is found in Fig. 4 that the susceptance J increases rapidly with the number of finger at extremely low frequency (f < 1.5 GHz in this example). It actually indicates the lumped element characteristics of an IDC in the limiting case for which the total size of the IDC is much smaller than the operating wavelength. As frequency goes beyond this limiting point, the susceptance is strongly enhanced for $N < 8$ and it tends to be gradually saturated for $N = 10$. It suggests that the low-frequency lumped effects disappear as the total size (number) of fingers is increased to a certain value comparable with the operating wavelength. The symmetry of structure and even number of finger yields two identical electrical lengths. Also, Fig. 4 shows the linear phase behavior for different N versus frequency except for a minor nonlinear disturbance for large N due to its distributed effect.

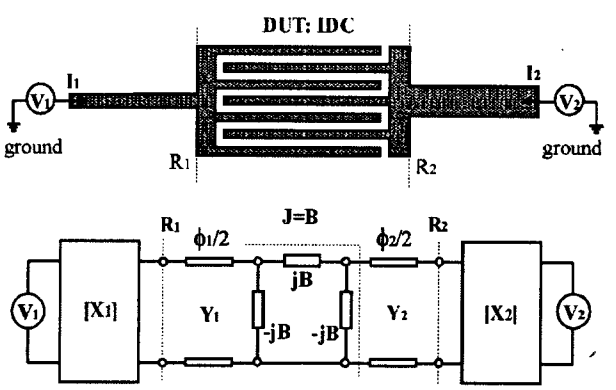


Fig.3: Physical topology and J-inverter network of a microstrip IDC attached with two different lines.

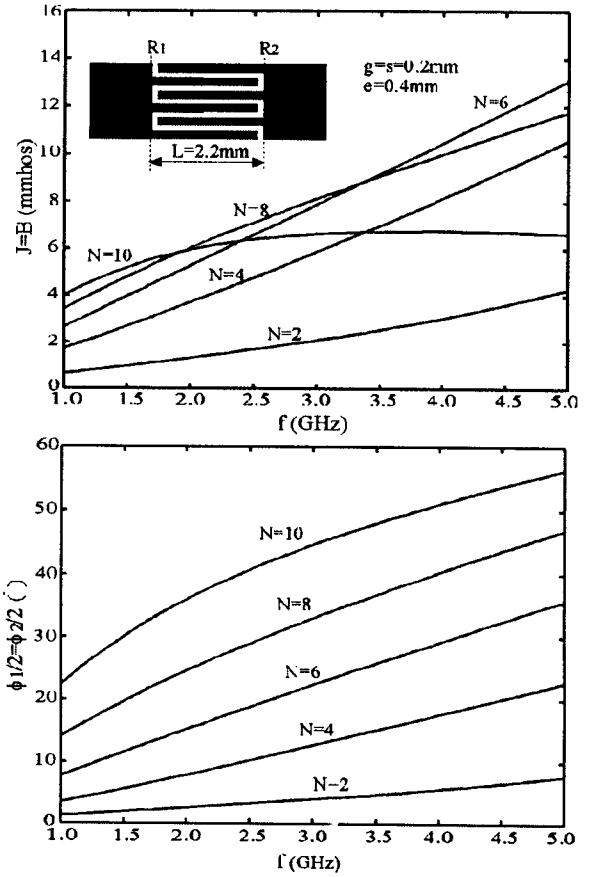
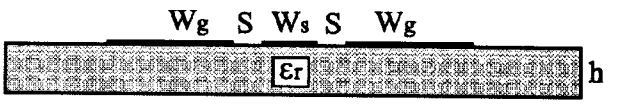
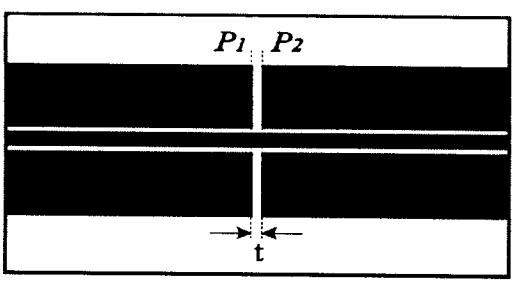


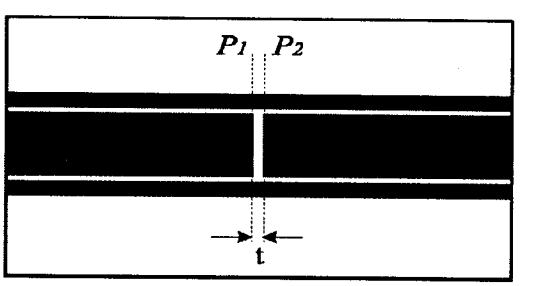
Fig. 4:Extracted network parameters of J-inverter for a microstrip IDC structure.



(a) cross-section of FGCPW line

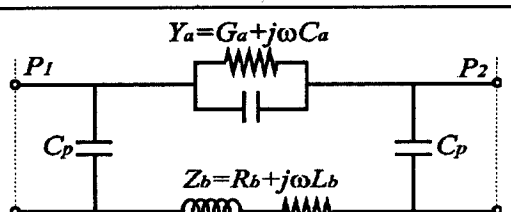


(b) FGCPW capacitive element: class (A)

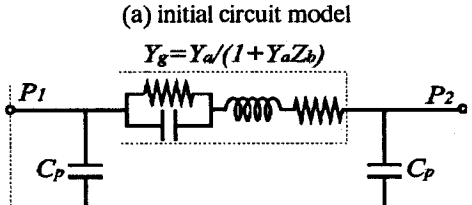


(c) FGCPW capative element: class (B)

Fig. 5: Layout view of finite-ground coplanar waveguide (FGCPW) capacitive series elements.



(a) initial circuit model



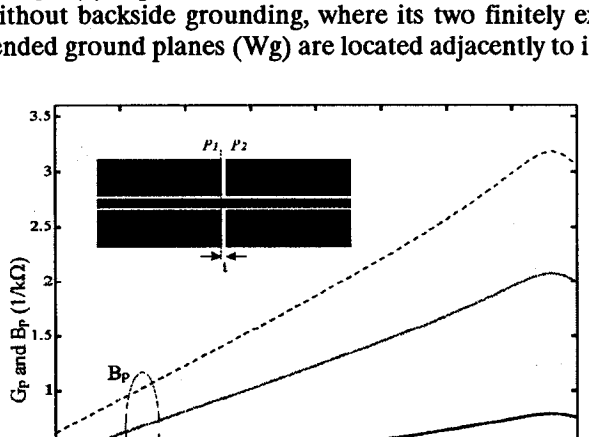
(b) modified circuit model

Fig. 6: Unified CAD-oriented circuit model of FGCPW capacitive series elements.

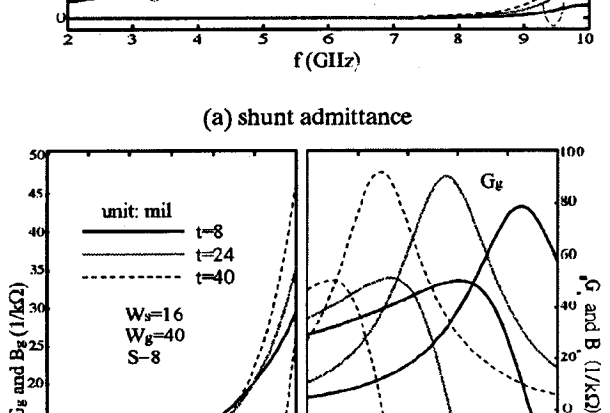
(B) FGCPW CAPACITIVE ELEMENTS

Fig. 5(a) depicts the cross-section of an FGCPW line without backside grounding, where its two finitely extended ground planes (Wg) are located adjacently to its central strip conductor (Ws). Fig. 5(b) and (c) show a schematic layout of the two classes of FGCPW capacitive series-connected elements to be studied. As opposed to their conventional CPW structure, the FGCPW elements have an additional degree of design freedom for the realization of a pre- designated series reactance in uniplanar circuits. With the finite extent of the two ground planes, those FGCPW elements can be designed by splitting longitudinally the ground planes of uniform FGCPW line to make up a gap structure, as in Fig. 5(b). Also, the capacitive element can also be realized by applying this scheme to the signal strip with finite width, as in Fig. 5(c).

Fig. 6(a) depicts the initial circuit model for FGCPW series-connected (gap) capacitive structures as in Fig. 5(b) and (c). This model consists of two shunt capacitors (C_p) and a pair of parallel capacitive admittance ($Y_a = G_a + j\omega C_a$) and inductive impedance ($Z_b = R_b + j\omega L_b$) at the two reference planes, P_1 and P_2. Such a circuit topology is different from that of a microstrip or CPW gap structure that has electrically infinite extended ground planes. In this case, Z_b represents an additional inductive parameter caused by the finite extent of signal- or ground-strip widths if the other strip is gap- discontinued. Further, this original model can be converted into its more convenient format, as shown in Fig. 6(b),

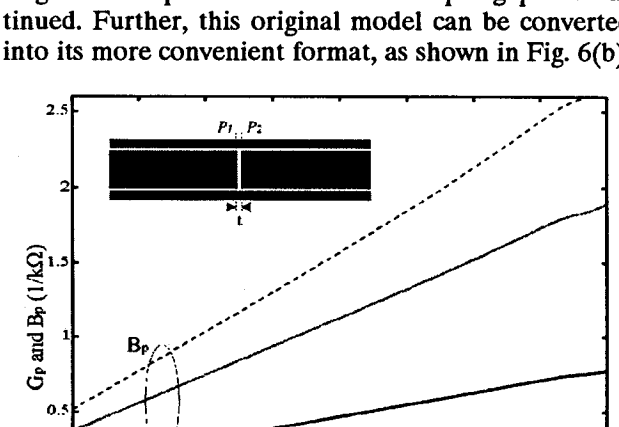


(a) shunt admittance

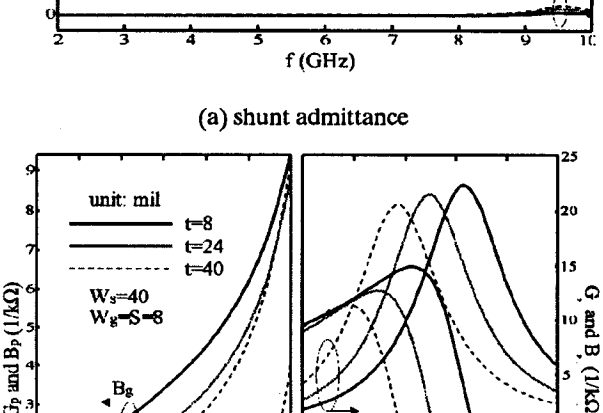


(b) series admittance

Fig. 7: Extracted equivalent circuit parameters of wide-ground FGCPW capacitive element: class (A).



(a) shunt admittance



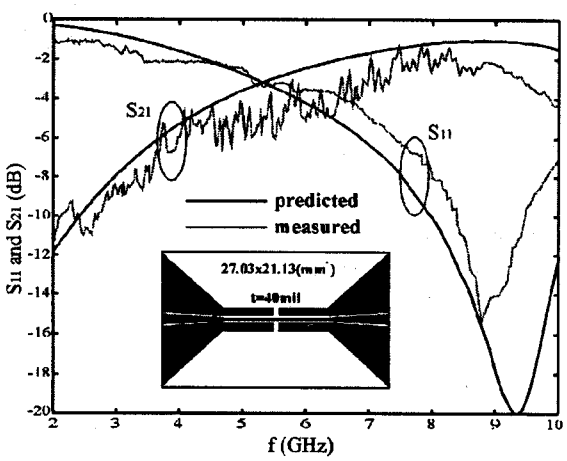
(b) series admittance

Fig. 8: Extracted equivalent circuit parameters of wide-ground FGCPW capacitive element: class (B).

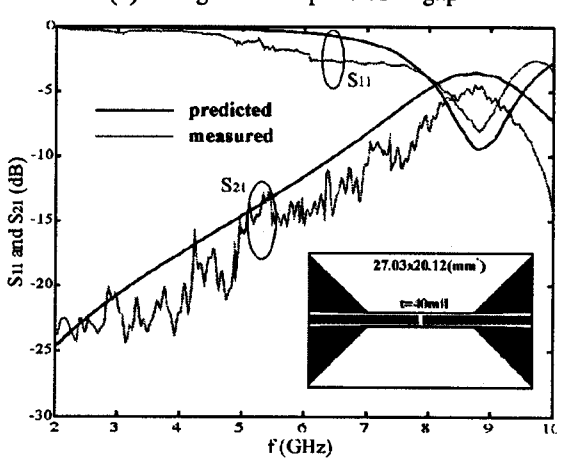
where the capacitive Y_a and inductive Z_b are put together to make up a series lossy RLC resonator sandwiched between the two FGCPW open-ends. The lossy factor is related to potential radiations generated by electric field distributed inside the gap region and also current density flowing along the continuous signal- or ground-line section.

Special attention is focused on the modeling characterization of the two FGCPW structures that have wide ground-strip gap and wide signal-strip gap. They are usually responsible for more significant coupling strength and more serious resonant behavior. Fig. 7 and Fig. 8 give a set of SOC-calibrated frequency-dependent lumped elements of the above described circuit model. To highlight resonance characteristics at high frequencies, the complete curves for Y_g ($Y_g = G_g + jB_g$) are plotted over the two differently scaled frequency ranges (*2.0 - 8.0 GHz*) and (*8.0 - 10.0 GHz*), as shown in Fig. 7(b) and Fig. 8(b). Generally, the extracted two shunt capacitances (C_p) are found to be virtually frequency- independent within the noted frequency range (*2.0 - 10.0 GHz*) while they are negligible over the frequency range of interest in the circuit model.

On the other hand, Fig. 7(b) and Fig. 8(b) indicate that the series susceptance (B_g) behaves quasi-linearly in the low frequency range and then an abrupt increment occurs as frequency increases further. The series conductance (G_g) is extremely small at low frequency and then it goes up rapidly. As frequency increases further, B_g drops quickly while G_g is raised to a certain maximum value, thus suggesting the existence of a RLC resonance phenomenon. If the gap distance (t) becomes shortened, B_g is slightly shifted up at low frequency, thereby showing that its coupling is enhanced to a certain extent. Nevertheless, the resonant frequency appears to move downward, which indicates a significant increase of the series inductance (L_b) and the series capacitance may remain intact (C_a). This is mainly brought from an inductive (signal- or ground-) strip line section with the narrow width, around the air-gap region.



(a) wide ground-strip FGCPW gap



(b) wide signal-strip FGCPW gap

Fig. 9: Predicted and measured results for the two FGCPW capacitive series structures, driven by two tapered 50 Ω FGCPW lines.

To verify our proposed model and the above-discussed properties, the two FGCPW gap structures are fabricated and measured. They are realized with t = *24mil* with tapered 50 Ω CPW lines at the two sides of the circuits that facilitate measurements with our network analyzer. Extracted return and insertion losses are plotted together with measured results as shown in Fig. 9, showing a good agreement. This is also to confirm well our claimed existence of the "resonance" behavior at high frequency. In fact, radiation loss around the resonant frequency is too significant to be ignored in the extracted circuit model. Given that gap distance *t=24mil*, the insertion loss (S_{21}) in Fig. 9(a) is found much higher than that in Fig. 9(b), which indicates a large enhancement of capacitive coupling by using an FGCPW wide ground-strip gap. This coupling behavior can easily be understood by comparing two groups of our SOC-extracted series susceptance (B_g), as shown in Fig. 8(b) and Fig. 8(b).

VI. CONCLUSION

This paper presents a new numerical de-embedding technique, "short-open calibration" (SOC) that is self-consistently formulated in the 3-D MoM, towards a universal parametric extraction of planar ICs. With the SOC scheme, an unbounded planar discontinuity can be characterized as its unified dynamic circuit model. This is in particular appealing for computer-aide design (CAD) and optimization of multilayered M(H)MICs and planar antennas. The SOC effectively extracts the truly realistic circuit parameters with two sets of numerical standards. It is done through the removal of any parasitic effects from the circuit model through a network segmentation procedure.

In this work, circuit models for MS interdigital capacitor (IDC) and FGCPW discontinuities are effectively extracted and presented. They are well confirmed by our measurements over a wide frequency range. The proposed SOC technique and unified circuit model are very useful in bridging the gap between the application-oriented CAD/optimization and field-theoretical modeling/analysis.

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