Silicon Chips for GSM Base Station Receivers

Olga Boric-Lubecke, Jenshan Lin, Penny Gould[1]

Abstract - **This paper describes silicon RFIC's designed for GSM900/DCS 1800 base station receivers. GSM standard and radio requirements are reviewed, and circuits that meet those requirements are discussed. A low-phase noise VCO, a high linearity low noise amplifier, a high linearity mixer, and a low-residual phase noise buffer amplifier, all fully integrated in 0.25um BiCMOS technology, are presented. Performance of these circuits demonstrated that it is feasible to use low cost silicon technology for base station receiver radios.**

Keywords - **Silicon RFIC's, BiCMOS technology, base station receivers, GSM specifications.**

I. INTRODUCTION

Global System for Mobile communications (GSM) specifications for Base Transceiver Stations (BTS's) impose challenging requirements for the whole receiver front end, in comparison with mobile stations (MS) [1]. While handsets handle only one channel at a time, a base station receiver handles multiple channels and cannot use gain control to increase its dynamic range. Therefore base station receivers typically require more stringent circuit performance than receivers used in handsets.

A receiver's reference sensitivity, intermodulation characteristics, and blocking characteristics set stringent requirements on the performance of individual components of a typical receiver front end. Figure 1 shows the most commonly used heterodyne receiver front-end architecture. It would be desirable to have as many of these components as possible integrated in low cost silicon technology, to reduce both the cost and size of the BTS. While there is no compact, integrated solution for filtering components available today, other components could in principle be integrated on a single chip. Mobile receivers that meet GSM requirements have already been implemented in low cost silicon technology [2], however base station receivers are typically still realized in GaAs technology [3].). Even though silicon RFIC technology is steadily improving, it is still a challenge to achieve noise figure (NF), phase noise, and linearity requirements for BTS applications with presently available devices.

O. Boric-Lubecke and J. Lin are with Bell Labs, Lucent Technologies, 600 Mountain Ave., Murray Hill, NJ07974, USA.

P. Gould is with Bell Laboratories, Lucent Technologies, Swindon, UK.

Performance of silicon IC's is limited both by active as well as passive devices. Passive devices typically outnumber active devices in RFIC's, and also occupy most of the chip area. Planar spiral inductors are probably the most commonly used, and discussed, passive components. Low quality factor (Q) of these inductors can significantly degrade circuit performance, such as VCO's phase noise when used in an on-chip resonator or LNA's NF when used for input matching.

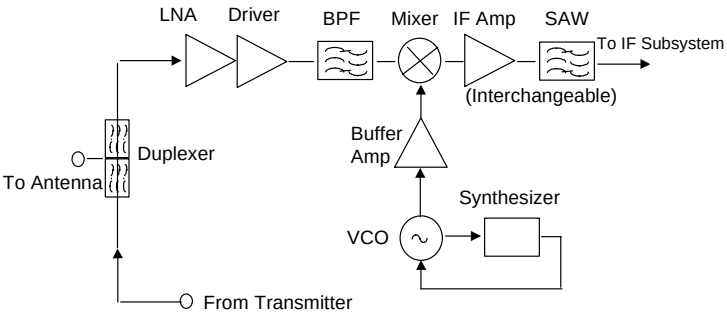


Fig. 1 Typical BTS receiver front-end architecture.

Choice of bipolar versus CMOS devices depends on the available process, and the particular component that is to be designed. For example, bipolar devices have a lower 1/f noise than CMOS devices, and are therefore a more suitable candidate for a low phase-noise circuit such as VCO. On the other hand, CMOS devices typically exhibit a lower NF_{min} (less than 0.5 dB) than bipolar devices in BiCMOS technology, and are therefore most likely a better choice for LNA design, even though bipolar devices might be suitable as well.

Proper partitioning of the NF, linearity and gain requirements among the front-end components is also an important issue. While the LNA dominates contributions to the NF of the system, receiver linearity is dominated by the mixer performance. The gain of the LNA should be just sufficient to meet the NF requirement, so that the linearity requirement on the mixer can be relaxed. On the other hand, IF amplifier gain can be adjusted to a higher value if necessary, with smaller penalty on the overall linearity of the front end.

In this paper we will discuss the feasibility of implementing a GSM BTS receiver in silicon-MMIC 0.25 μm BiCMOS process. Initialy, GSM standard as well as radio requirements are reviewed. Base station receiver sensitivity, linearity and phase noise specifications are derived and compared to those for mobile stations. Next, silicon RFIC's that meet those requirements for GSM900/DCS1800 base station receivers are presented. The receiver chips achieve low noise figure and high third order intercept (IP3) simultaneously without any gain control. The chips were fabricated using a 0.25μm BiCMOS process with inductor quality factor (Q) of approximately 10. With a supply voltage of 3V, current consumption is 132mA for the GSM900 receiver and 117mA for the DCS1800 receiver. This was the first reported silicon-integrated radio front end for base stations [4].

II. GSM STANDARD

GSM is currently the most widely used digital cellular radio system. As of June 2001 [5], there are over 550 million GSM users, accounting for two thirds of world users. In contrast, second most popular standard, CDMA, has only about 96 million users. GSM provides international roaming capability, which is currently available in 171 countries.

GSM standard is based on a time-division-miltiple access (TDMA) and frequency-division-multiple access (FDMA) scheme, and it uses Gaussian Minimum Shift Keying (GMSK) modulation. Channel bandwidth is 200 kHz, and each channel is shared by 8 users in a TDMA mode. It uses a full duplex communication, in three frequency bands: 900 MHz, 1800 MHz, and 1900 MHz. Digital cellular system (DCS) 1800 MHz band was introduced in Europe in early 1990's to provide more bandwidth. Personal communications services (PCS) 1900 MHz band is used in the US. GSM bandwidth allocations are summarized in Table I.

TABLE I
GSM FREQUENCY ALLOCATIONS

	GSM900	DCS1800	PCS1900
f(MS Tx-BTS Rx) [MHz]	890-915	1710-1785	1850-1910
f(BTS Tx-MS Rx) [MHz]	935-960	1805-1880	1930-1990

GSM is a second generation (2G) cellular standard, which will gradually be replaced by a third generation (3G) UMTS standard. 3G standards are currently being developed across the industry and by global groups such as the Third Generation Partnership Project (3GPP). 3G services will offer enhanced capacity, quality and data rates, which will enable high speed multimedia and internet access. Even though 3G systems will offer various services not available today, radio specifications will be similar to those required by 2G systems.

III. GSM RADIO SPECIFICATIONS

GSM base station and mobile radio receiver requirements, referenced at the antenna connector, will be derived from the GSM specification 05.05 document [1]. Values obtained for noise figure (NF), linearity and phase noise should be considered as reference values only. Vendors typically design their products to exceed these values by a certain margin to give them a competitive advantage.

A. Noise Figure

Receiver NF can be determined from reference receiver sensitivity (S) [1], knowing the input noise floor, and signal to noise ratio (SNR) requirement. Noise floor (N) can be determined from the Nyquist equation for thermal noise:

$$N = kTB, \quad (1)$$

where k is a Boltzman constant, T is the temperature in Kelvins, and B is the single-sided noise bandwidth of the system. At room temperature, T=290K, noise power per bandwidth can be calculated to be –174 dBm/Hz. In the case of a GSM receiver, channel bandwidth is 200 kHz, resulting in a noise floor of –121 dBm. The SNR depends on the bit-error-rate (BER) required for digital radio quality and the implementation of baseband algorithms. For example, a frequency hopping system can reduce the SNR requirement from 11 dB to 9 dB [6]. For given reference receiver sensitivity S, maximum noise figure can be calculated as:

$$NFmax = (S-SNR) - N \quad (2)$$

Table II shows the receiver sensitivity and NF requirement assuming SNR of 9 dB. Due to a lower reference sensitivity, a 2 dB lower NF radio is required for normal base stations than for mobile devices. Normal BTS has the lowest receiver NF specification of 8 dB, which after system partition results in a LNA NF requirement of under 2 dB.

TABLE II
RX FRONT-END NF REQUIREMENTS

	GSM 900 Small MS	DCS 1800 MS	GSM 900 Micro BTS	DCS 1800 Micro BTS	GSM 900 Normal BTS	DCS 1800 Normal BTS
Reference Sens[dBm]	-102	-102	-97	-102	-104	-104
NF [dB]	10	10	15	10	8	8

B. Linearity

Receiver intermodulation characteristics determine linearity requirements (third-order intercept point or IP3) for the front end. According to GSM standard [1], reference sensitivity performance should be met when the following three signals exist simultaneously at the input of the receiver: (1) a wanted signal at frequency f_o 3dB above the reference sensitivity, (2) a CW interfering signal at 800 kHz offset from f_o, and (3) a modulated interfering signal at 1600 kHz offset from f_o, as shown in Fig. 2. Two interfering signals should be of the same strength (Table III).

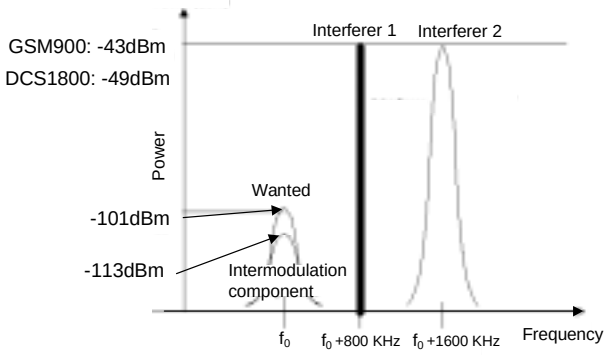


Fig. 2 GSM intermodulation characteristic

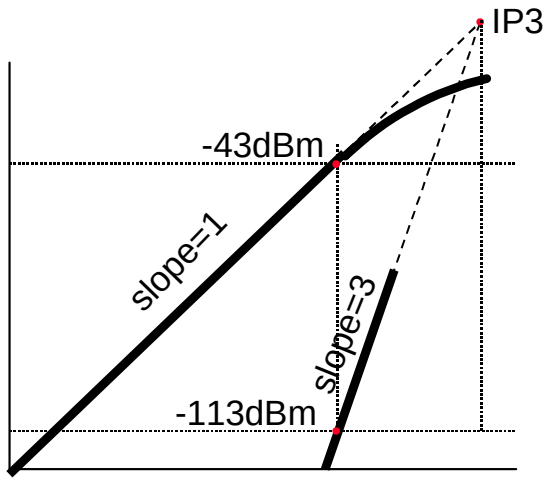


Fig. 3 Third-order intercept point for GSM normal BTS.

For example, GSM900 normal BTS reference sensitivity is –104 dBm. Therefore wanted signal should be at –101 dBm, and interferers are specified to be –43 dBm. Intermodulation component, combined with noise, should be SNR lower than the wanted signal. Assuming that intermodulation component and noise have the same power, we arrive at the conclusion that intermodulation component should be –113 dBm. Once interferer (P_{test}) and intermodulation (I) power levels are known, it is straight forward to calculate input IP3 (IIP3), using diagram in Fig. 3:

$$IIP3 = P_{test} + 0.5 \times (P_{test} - I) \quad (3)$$

Interferer levels specified in [1], and corresponding IIP3 are shown in Table III. Since there is less attenuation at the air interface at 900 MHz than at 1800 MHz, 900 MHz BTS interferers are specified 6dB higher than for DCS 1800 BTS, and resulting IIP3 requirement will be significantly more stringent. After system partition, and depending on the front-end configuration, these requirements results in a mixer specification for IIP3 of 15-20 dBm, while keeping conversion loss under 8 dB so that the NF is not degraded.

TABLE III
RX FRONT-END INPUT IP3 REQUIREMENTS

	GSM 900 Small MS	DCS 1800 MS	GSM 900 Micro BTS	DCS 1800 Micro BTS	GSM 900 Normal BTS	DCS 1800 Normal BTS
Interferer [dBm]	-49	-49	-43	-49	-43	-49
IIP3 [dBm]	-18	-18	-10	-18	-8	-17

C. Phase Noise

The difficult phase noise requirement for the VCO comes from the in-band blocking characteristics. Based on the reference sensitivity, the blocking requirement, and the assumption of C/I = 9dB, the phase noise specifications were calculated and summarized in Table IV [7]. GSM 900 micro and normal BTS have the most stringent phase noise requirement, as is the case for IIP3 requirement. Phase noise specifications are over 10 dB lower for normal BTS than for MS at 1800 MHz, and close to 20 dB lower at 900 MHz.

TABLE IV
VCO PHASE NOISE REQUIREMENT [dBC/HZ]

Offset [kHz]	GSM 900 Small MS	DCS 1800 MS	GSM 900 Micro BTS	DCS 1800 Micro BTS	GSM 900 Normal BTS	DCS 1800 Normal BTS
600	-118	-116	-130	-121	-137	-128
800	-118	-116	-140	-131	-147	-138
1600	-128	-126	-140	-131	-147	-138
3000	-133	-133	-140	-131	-150	-138

IV. RFIC IMPLEMENTATION

Agere (formerly Lucent Microelectronics) BiCMOS process described in [8] was used for this work. It is a CMOS-based BiCMOS technology, optimized for high-speed CMOS devices. Bipolar devices were fabricated using a low-cost, four-mask process integrated as a module in 0.25 μm core CMOS technology. These devices yielded f_t > 30 GHz and f_{max} > 25 GHz, for emitter size of 2.88μm^2. Five metal levels are available in this process, with 3μm thick top level metal for improved inductor Q. Typical planar spiral inductor Q values achieved using this process, for inductance of 1-10 nH, are around 10. Measured inductance and Q values for 3 nH and 5 nH inductors are shown in Fig. 4.

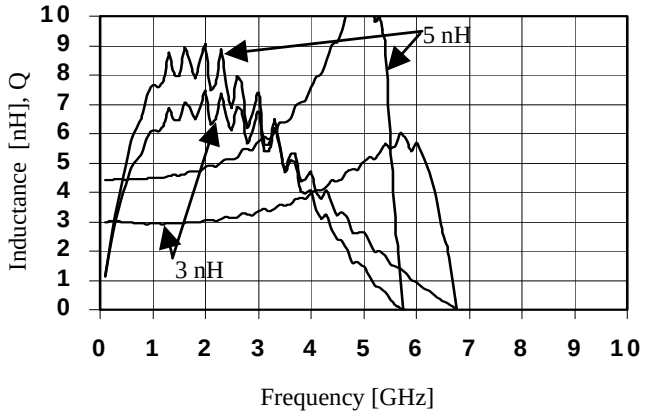


Fig. 4 Measured inductance and Q values for 3 nH and 5 nH planar spiral inductors.

Fully integrated bipolar oscillator realized in this technology was reported in [7]. Phase noise at 600 kHz, 800 kHz, 1.6 MHz, and 3 MHz offset frequencies was measured to be –129 dBc/Hz, -132 dBc/Hz, -142 dBc/Hz, and –148 dBc/Hz, respectively. This phase noise performance meets the DCS 1800 MS, GSM 900 small MS (handset with output power less than 2W), and DCS 1800 Micro BTS requirements, and comes very close to meeting DCS 1800 normal BTS requirement. Among integrated VCO's with on-chip resonators in a silicon-based process, this is the lowest phase noise reported to date [7].

The block diagram of the RF receiver is shown in Figure 5. The LNA before mixer is partitioned into LNA1 and LNA2. The input to LNA1 is connected to duplexer. A switch between LNA1 and LNA2 is needed for loop test once the chip is mounted in the system. The output of LNA2 goes to a 3dB power divider of which one output is used for diversity while the other goes back on chip after a dielectric filter. The dielectric filter is used to reject image band noise and other out-of-band interference. The on-chip balun converts single-ended input to differential signal for the balanced mixer. The on-chip LO buffer converts single-ended LO input to differential output and amplifies its power level to drive the double balanced mixer. IF port of the mixer goes to the IF buffer before a SAW filter or IF sampling. All of the building blocks are integrated in a 0.25μm silicon BiCMOS process except the 3dB power divider and the dielectric filter. All of the RF inductors required in the circuits are integrated on-chip.

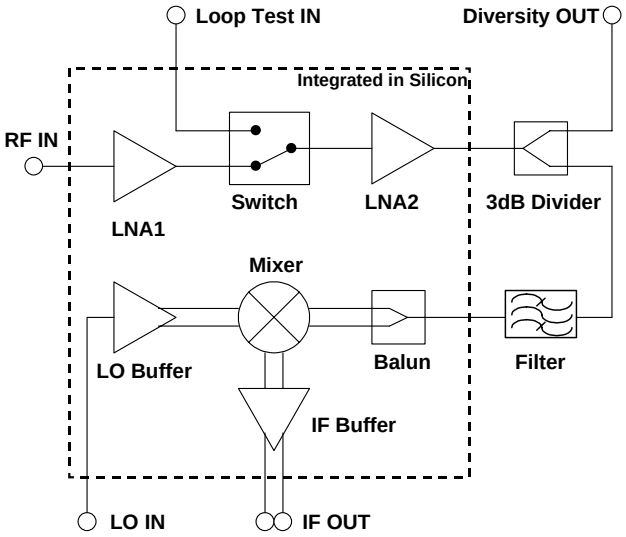


Fig. 5 BiCMOS receiver block diagram.

The partition of gain, noise figure, and IP3 is optimized to achieve the best overall performance. LNA1 and LNA2 have similar structure except LNA1 is optimized for low noise figure and LNA2 is optimized for high IP3. This is done by optimizing the bipolar transistor size, operating current, and degeneration inductance. The switch between LNA1 and LNA2 not only functions as a loop-test switch, but also has a variable attenuation control that can be used to adjust overall receiver noise figure and linearity. A simplified schematic consisting of LNA1, switch, and LNA2 is shown in Figure 6. The LNA1 achieves noise figure under 2dB at both bands, whereas LNA2 achieves output IP3 greater than 22dBm at both bands.

V. CIRCUIT PERFORMANCE

A. LNA

A single stage, common emitter configuration was chosen for both LNA1 and LNA2 amplifiers in each band, in order to achieve high linearity and low NF [9]. Emitter sizes of 76.8 μm^2 at 900 MHz and 49.92 μm^2 at 1800 MHz were chosen to yield good NF, and gain at the design frequency. On-chip impedance matching with inductors at the input was avoided, since any extra loss at the input would increase the noise figure. Degeneration inductance was used in the emitter, to improve input and output return losses, and to increase IIP3.

Although LNA1 and LNA2 were designed to have similar gain, in link budget partition, LNA1 was optimized for low noise figure and the driver for high IIP3 [10]. In the GSM900 receiver, LNA1 has 1.4dB noise figure, 13 dB gain and 9.3 dBm input IP3 while LNA2 has 2.5 dB noise figure, 9.6 dB gain and 17 dBm input IP3. In the DCS1800 receiver, LNA1 has 1.9dB noise figure, 11.3 dB gain and 3.7 dBm input IP3 while LNA2 has 2.1 dB noise figure, 12.2 dB gain and 10.7 dB input IP3. A collector bias current of 13 and 11 mA was used for LNA1 in GSM900 band and DCS1800 band, respectively; 33 and 22 mA was used for LNA2 in GSM900 band and DCS1800 band, respectively.

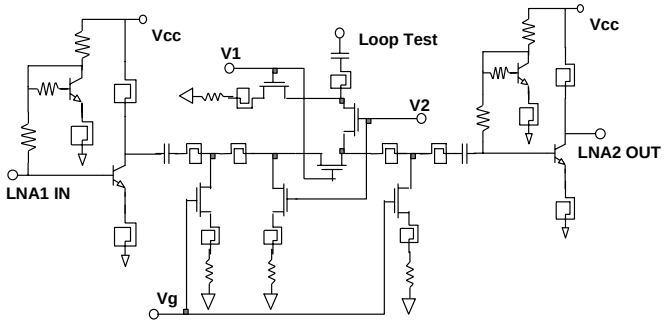


Fig. 6 Simplified schematic of LNA1, switch and LNA2.

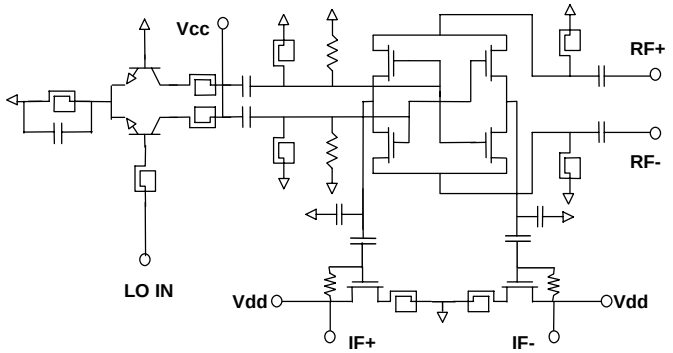


Fig. 7 Simplified schematic of mixer, LO buffer, and IF amplifier.

B. Mixer

To achieve the best receiver noise figure and linearity simultaneously, a resistive CMOS mixer is used. This type of mixer has very high input IP3 compared with other mixer types [11]. Traditionally, such a mixer has been implemented using GaAs FET devices. However, a resistive mixer using silicon MOSFET can achieve same performance with much lower cost. In addition, it requires no DC bias. The resistive CMOS mixer has a double balanced ring structure and has broadband performance [12]. The CMOS mixer used here has conversion loss better than 6.5 dB at both bands. It achieves very high input IP3 at 18.9 dBm and 21.9 dBm at 900 MHz and 1800 MHz, respectively. The mixer used an IF of 170 MHz and total LO power drive of 14 dBm. This mixer has demonstrated a wide band of operation and graceful degradation in conversion loss of 1.3 dB or less over a falling LO power level of 14 dBm to 4 dBm. LO to IF isolation of 43 dB, and RF to IF isolation of 29.5 dB were measured at a LO power of 14 dBm. IF port return loss was measured to be –15.5 dB, with RF return losses of approximately 10 dB. This mixer has the lowest conversion loss and highest associated input IP3 reported to date for passive CMOS mixer MMICs within its frequency bands [12]. The LO power level requirement of 14 dBm, enables this mixer to be realistically driven from a CMOS buffer amplifier.

C. LO Buffer Amplifier

Since the resistive mixer requires high LO drive, a linear buffer amplifier at the LO port is integrated on-chip. The LO buffer also functions as an active balun that converts a single-ended LO signal to a differential LO signal. Its Output P_{1dB} is greater than 13 dBm with phase balance error of less than 2 degrees. To maintain the LO signal purity and meet the GSM blocking test requirement, the LO buffer should have low residual phase noise performance. The measured residual phase noise is less than –155 dBc/Hz at offset frequencies 100kHz and above [13]. Since VCO operates in a large-signal mode, to achieve lower phase noise, it generates undesirable higher harmonics that are filtered in the buffer amplifier. Buffer amplifier can be operated from 1.5 V to 5 V, with its phase and amplitude balance error within 5° and 2dB. At 5 V supply, bias current is 65 mA, and the circuit has phase and amplitude balance error less than 2° and 1.2 dB, respectively. Noise figure varies between 5.6 dB and 5.9 dB for bias voltage from 1.5 V to 5 V. Gain is about 6 dB at both outputs, while the attenuation is over 30 dB for frequencies above 4 GHz. The circuit demonstrated the feasibility of achieving both good signal balance and high dynamic range in an active balun with a simple topology [13].

D. IF Amplifier

An IF buffer is connected after the mixer to compensate for the conversion loss of the mixer. Very high IP3 is also required for the IF buffer. By optimizing its transistor size and bias current, the IF buffer achieves 1.3 dB noise figure, 15.8 dB gain, and 13.1dBm input IP3 with a current of 40 mA. Both bandwidth of the mixer IF port and the bandwidth of the IF buffer amplifier are greater than 300 MHz. A simplified schematic consisting of mixer, LO buffer, and IF buffer is shown in Figure 7.

VI. RECEIVER PERFORMANCE

In the integrated receivers, bipolar transistors are used for LNA1, LNA2, and LO buffer whereas CMOS transistors are used for switch, mixer, and IF buffer. The bipolar transistor is chosen for its low noise behavior (both 50 Ω noise figure and 1/f noise) whereas CMOS transistor is needed for linearity. The chip layout is designed to fit into a TQFP-48 package with 7 mmx7 mm body size. Both chips have a similar size of about 3.5 mm x3.5 mm.

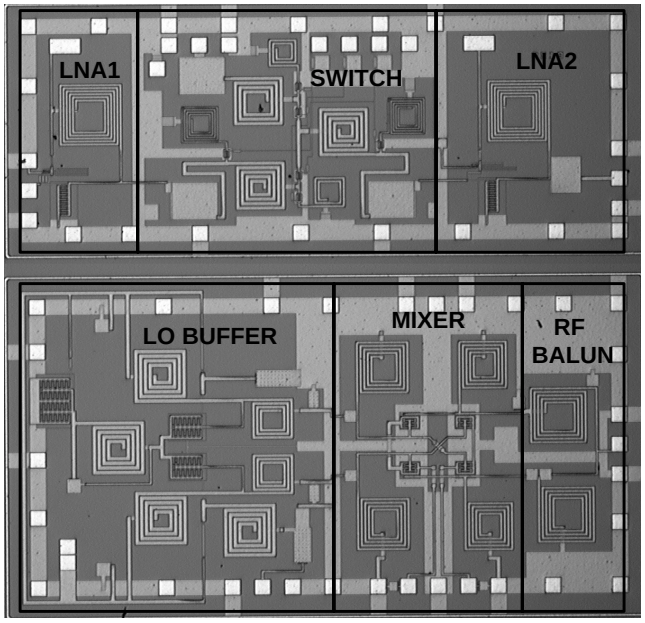


Fig. 8 DCS1800 receiver photograph. Chip size is 3.5mmx3.5mm.

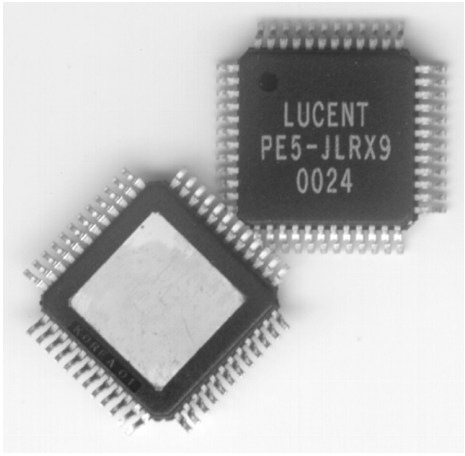
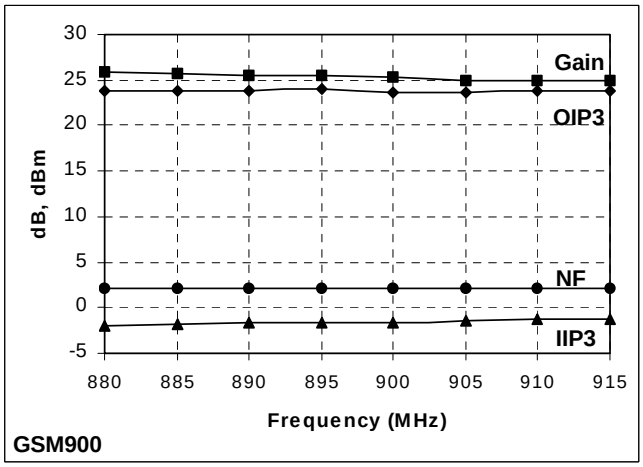
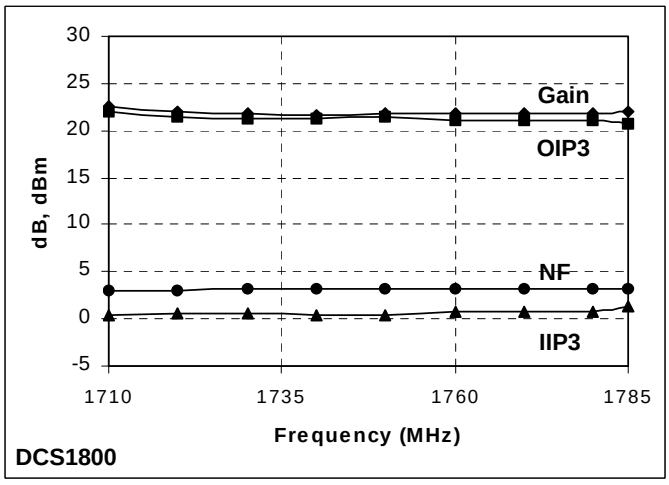


Fig. 9 Photograph of a packaged GSM900 receiver. Exposed pad package is used to minimize ground inductance.

To reduce the ground inductance and improve the performance, the ExposedPad™ TQFP-48 package is used [14]. The package has a backside ground pad that provides a very good RF ground to the chip. With a number of ground bond wires directly bonded to the ground pad, the total ground inductance is reduced to below 0.5 nH. Since the chip size is limited in this package, the CMOS IF buffer amplifier is packaged separately. This also allows the reuse of IF amplifiers after channel selection SAW filters to optimize overall system sensitivity. The die photo of DCS1800 integrated chip including LNA1, switch, LNA2, mixer, RF balun, and LO buffer is shown in Figure 8, and packaged GSM900 chip in Figure 9. The GSM900 integrated chip is similar in layout to DCS1800 chip.



(a)



(b)

Fig. 10 GSM900 (a) and DCS1800 (b) receiver performance.

The integrated receivers achieve better than 2.1dB noise figure, 25.3dB gain, -1.9dBm input IP3 in the GSM900 band and better than 3.3dB noise figure, 20.7dB gain, and 0.4dBm input IP3 in the DCS1800 band. The frequency responses of both receivers are shown in Figure 10. Both receivers show a

flat response over their respective bandwidth. A summary of each receiver performance, as well as individual circuits is shown in Figure 11. The building blocks were tested on-wafer and the integrated receivers were tested in packages. These chips were the first silicon RFIC's developed for base station receivers. The measured results demonstrates the feasibility of making compact and low-cost transceiver units for base station applications, which is essential to the hardware implementation of 3G wireless communication systems utilizing multiple antennas and front end radios to increase capacity.

GSM900 Receiver	NF (dB)	Gain (dB)	P_{1dB} (dBm)	IIP3 (dBm)	OIP3 (dBm)	Current (mA)
LNA1	1.4	13.0	-5.5	9.3	22.3	12.9
LNA2	2.5	9.6	3.0	17.0	26.0	32.9
Broadband Switch	2.2	-2.2	17.5	30	27.8	0
Mixer w/ LO Buffer	6.3	-6.3	10.3	18.9	12.6	45.8
IF Buffer	1.3	15.8	2.0	13.1	28.9	40
Integrated Receiver	2.1	25.3	-8.2	-1.9	23.6	132

DCS1800 Receiver	NF (dB)	Gain (dB)	P_{1dB} (dBm)	IIP3 (dBm)	OIP3 (dBm)	Current (mA)
LNA1	1.9	11.3	-9.0	3.7	15.0	10.7
LNA2	2.1	12.2	-3.0	10.7	22.9	22.1
Broadband Switch	3.3	-3.3	18.5	27	23.7	0
Mixer w/ LO Buffer	6.4	-6.4	11.3	21.9	15.5	44.6
IF Buffer	1.3	15.8	2.0	13.1	28.9	40
Integrated Receiver	3.3	20.7	-9.0	0.4	21.6	117

Fig. 11 GSM900 and DCS1800 receiver and individual circuit performance summary.

VII. Conclusions

GSM 900/DCS 1800 BTS specifications present a challenge in terms of receiver front-end noise figure, linearity, and phase noise. These requirements are significantly more stringent for base stations than for handsets. Linearity and phase noise specification are particularly difficult for GSM900 normal base station. Even though these specifications are very difficult to achieve in silicon MMIC technology, it is possible to meet them with the optimum specification partition, device choice and layout, and circuit configuration. Choice of a resistive CMOS mixer was critical to achieve required linearity performance. Performance of a fully integrated BiCMOS radio receiver front-end described in this paper, demonstrates that it is feasible to meet GSM BTS specifications with low-cost silicon technology.

Acknowledgments

The authors would like to thank Lucent GSM group in Swindon, UK for collaboration, Agere (formerly Lucent Microelectronics) for chip fabrication, and R. Whitehouse from Agilent Technologies for providing testing equipment. Technical discussions with C. Zelley, V. Archer, Y-J. Chen, J. Clancy, V. Lubecke, T.-P. Liu, E. Westerwick, and chip layout by F. Hrycenko and T. Gabara are greatly appreciated.

References

[1] GSM 05.05 version 5.5.1 (ETS 300 910): "Digital cellular telecommunications system (Phase 2+); Radio transmission and reception," January 1998.

[2] M. Steyaert at all, "A Single-Chip CMOS Transceiver for DCS-1800 Wireless Communications," *IEEE ISSCC Digest of Technical Papers*, pp. 48-49, February 1998.

[3] T. Cameron at all, "A Multi-Chip Receiver Module for PCS1900 and DCS1800 GSM Basestations," *1999 IEEE Wireless Comm. And Networking Conf. Digest*, pp. 732-726.

[4] J. Lin, O. Boric-Lubecke, P. Gould, C. Zelley, Yung-Jin Chen, Y. Ran-Hong "3V GSM Basestation receivers using 0.25µm BiCMOS," IEEE ISSCC Digest of Technical Papers, pp. 416-471, February 2001.

[5] GSM World, www.gsmworld.com

[6] S. M. Redl, M. K. Weber, and M. W. Oliphant, "An Introduction to GSM," Artech House, 1995.

[7] J. Lin, "An Integrated Low-Phase-Noise Voltage Controlled Oscillator for Base Station Applications," *IEEE ISSCC Digest of Technical Papers*, pp. 432-433, February 2000.

[8] Y-F Chyan at all, "A 50 GHz 0.25µm Implanted-Base High-Energy Implanted-Collector Complementary Modular BiCMOS (HEICBiC) Technology for Low-Power Wireless-Communication VLSIs," *1998 IEEE Bipolar/BiCMOS Circuits and Technology Meeting '98, Conference Proceedings*, pp. 128-131, Minneapolis, September, 1998.

[9] L. E. Larson, "RF and Microwave Circuit Design for Wireless Communications," Norwood, MA, pp. 365-369, 1997.

[10] O. Boric-Lubecke, J. Lin, T. Ivanov, Y. Ran-Hong "Si-MMIC BiCMOS low-noise, high linearity amplifiers for base station applications," presented at APMC 2000, Sidney, Australia, December 2000.

[11] S. A. Maas, "Microwave Mixers", 2nd Edition, *Artech House*, 1993, pp.338.

[12] P. Gould, C. Zelley, and J. Lin, " CMOS Resistive Ring Mixer MMICs for GSM 900 and DCS 1800 Base Station Applications," *IEEE MTT-S International Microwave Symposium Proceedings*, pp. Boston, June 2000.

[13] J. Lin, C. Zelley, O. Boric-Lubecke, P. Gould, and R. Yan, "A silicon MMIC active balun/buffer amplifier with high linearity and low residual phase noise," *IEEE MTT-S International Microwave Symposium Proceedings*, pp. Boston, June 2000.

[14] Amkor ExposedPad™ TQFP Technical Data Sheet.