

# Miniature 6-18 GHz Switched-bit Phase Shifter

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**Abstract** – An extremely miniature 5-bit, 6-18 GHz, 25 nsec MIC switched-bit phase shifter has been developed. Both RF and the "on board" driver employ novel circuitry, which occupy only 280 square millimeter in a unique MIC configuration. Careful circuits layout to minimize leakage and coupling interaction supported with a 3D electromagnetic simulation lead to excellent RF performance, low cost design and a product which is compatible in size to a typical MMIC chip including it's supporting driver.

## I. INTRODUCTION

In today's modern microwave systems the need for low cost, high performance, small size and lightweight products keep motivate the designer for suitable solutions. MMIC chips [1] provide some answers to that; however, the heavy vendor dependency along with the uncertainty for future product support makes it unattractive. A need for an "in house" MIC solution lead to the development of this product.

High speed switched bit MIC phase shifter designs ranging from narrow band [2][3] and up to an octave band [4] are relatively straightforward; moreover, wider bandwidth [5] design result in a significant slower switching time response and lower power handling capability. This paper reports on the development of a novel approach to broadband, high frequency, ultra fast, miniature switched-bit phase shifter using a combination of hybrid coupled reflection circuitry and an I-Q vector modulator arrangement employing fast PIN diodes.

## II. PHASE SHIFTER DESIGN

The RF section of the phase shifter contains a switched - capacitor configuration for the three lower bits and a unique I-Q vector modulator structure for the two most significant bits connected in cascade. The switched - capacitor technique selected (Fig. 1) has relatively flat differential phase shift response over a large bandwidth ratio and only the 3 - dB quadrature hybrid employed limit it's performance.

The differential transmission phase shift of this structure equal to the differential reflection phase shift of the capacitance load when a high performance 3 – dB coupler is employed. Therefore, the synthesis simplifies to the reflection coefficient of the symmetrical capacitance loads, which are connected to a 3 – dB quadrature hybrid.

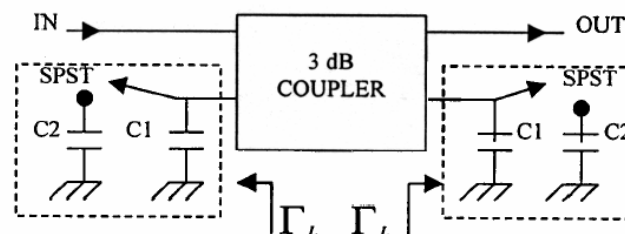


Fig. 1: Schematic of a typical switched - capacitor bit

The optimum response for each bit is when the capacitors C1 and C2 swing symmetrically around the J1 point on the perimeter of the Smith Chart. The average capacitance  $C_0$  that the capacitance C1 and C2 swing around it for each bit equals:

$$C_0 = \frac{1}{2\pi f_g Z_0} \quad (1)$$

Where  $f_g$  is the average frequency (geometrical mean) and  $Z_0$  is 50 ohms.

A straightforward mathematical manipulation of the reflection coefficient terms yields the following relationship:

$$C_1 = C_0 * K \quad \& \quad C_2 = C_0 / K \quad (2)$$

notice that

$$C_0 = \sqrt{C_1 * C_2} \quad \& \quad K^2 = \frac{C_1}{C_2} \quad (3)$$

where

$$K = \sec \frac{\theta}{2} + \tan \frac{\theta}{2} \quad (4)$$

and  $\theta$  is the desired differential phase shift at the average frequency.

The capacitance values and the differential phase shift flatness are summarized for each bit in the table below.

TABLE 1

PHASE SHIFT (Deg)	C1 (pF)	C2 (pF)	C1/C2	PHASE SHIFT FLATNESS (Deg)
11.25	0.338	0.278	1.216	1.50
22.5	0.373	0.251	1.486	2.95
45	0.458	0.205	2.234	5.53
90	0.739	0.127	5.819	8.21
180	$\infty$	0	$\infty$	0

<sup>1</sup> Authors are with EL T A Electronic Industries Ltd., P .O.B 330, Ashdod, Israel

It is evident from the above table that the three least significant bits require capacitance values that are of the same order of magnitude; In addition, printed capacitors on a ceramic substrate result in reasonable dimensions with respect to the wavelength at 18 GHz. Careful layout design is required to minimize radiation and coupling effects. Moreover, the presence of the SPST loads the reflection network and both the diodes and the biasing network have to be optimized for each bit. A novel biasing configuration was employed in order not to load the reflection network across the frequency range and yet not effect the switching time.

An I-Q vector modulator operating as a quadrature modulator is used for the two most significant bits. The I-Q vector modulator consist of an optimized two - section in phase two - way power divider to conserve space, wideband 3-dB quadrature hybrid and two proprietary bi - phase modulators as shown in Fig. 2.

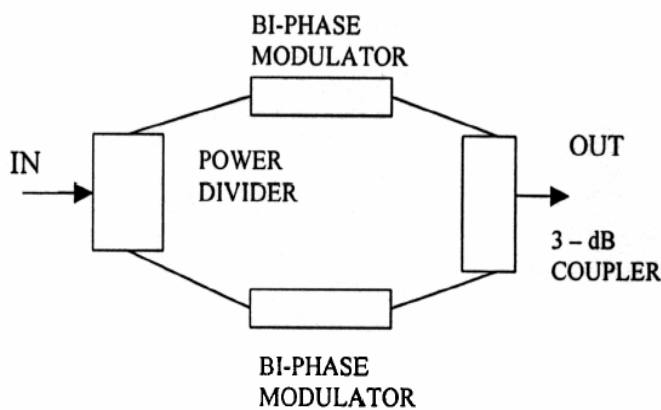


Fig. 2: I-Q Vector Modulator

Each bi-phase modulator contains four 3- dB quadrature hybrids connected in a double balance modulator configuration and employ fast PIN diodes that operate only at the ON/OFF mode for fast switching time and temperature stability reasons.

The intrinsic insertion loss of the I-Q vector modulator is therefore only 3 dB vs. the 6 dB for the slower speed and the finer resolution option (360 degrees range). It is possible to introduce the 45-degree bit within the I-Q vector modulator in the "switching mode" but at the expense of a 3-dB amplitude modulation, which is unattractive.

The driving logic sequence form a Gray code combination which gets translated into a TTL compatible interface using fast logic gates.

The entire design was realized on an alumina substrate for the following main reasons: Small size requirement, Lange coupler realization, high capacitance per unit area, temperature stability and low cost.

The drivers supporting all the bits are integrated on the same alumina substrate where all low frequency lines are carefully routed to minimize coupling interaction.

### III. PERFORMANCE

A prototype model of a 5-bit phase shifter operating in the 6-18 GHz band has been assembled and is shown in Fig. 3. Measured room temperature data are summarized in Fig. 4-8. This device uses a high speed driver and when operated as frequency translator it has a translation bandwidth of several megahertz. The relatively good carrier, sidebands and spurious suppression indicate that the phase and amplitude errors are relatively small. The phase to phase switching time is less than 25 nsec.

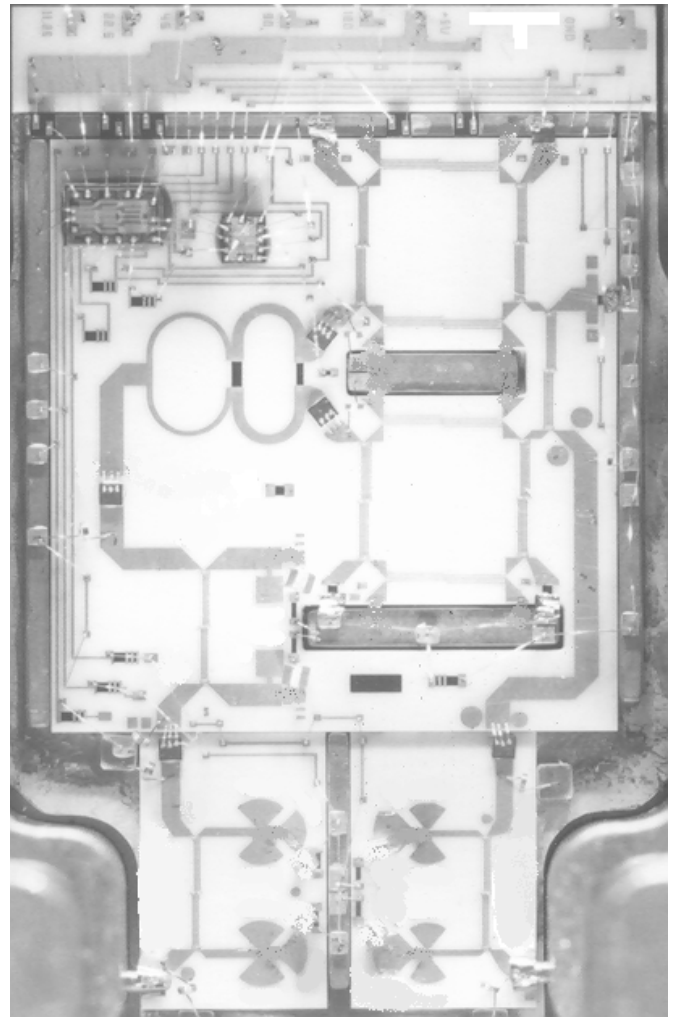


Fig. 3: 6-18 GHz, 5-bit Phase Shifter

The maximum power handling capability without performance degradation is +23 dBm. The device operates from a single +5V supply and consumes 180 mA. The performance over the temperature range of -55C to +95C is maintained as expected from the design and circuit implementation considerations.

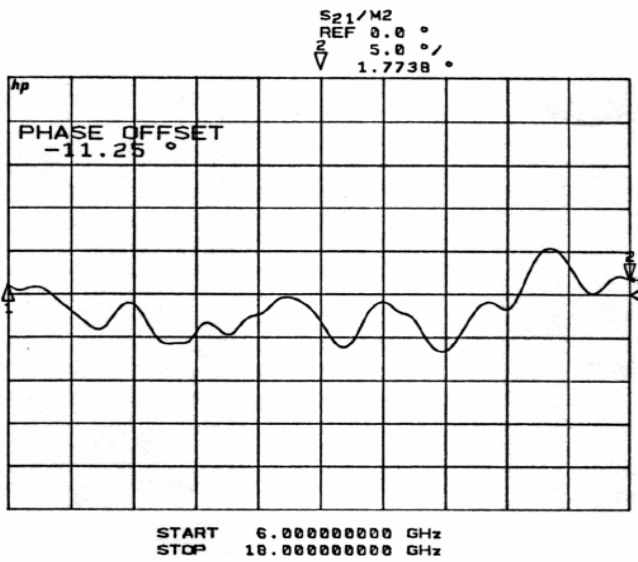


Fig. 4: Measured Phase Error of the 11.25-deg bit (representing the switched capacitor network)

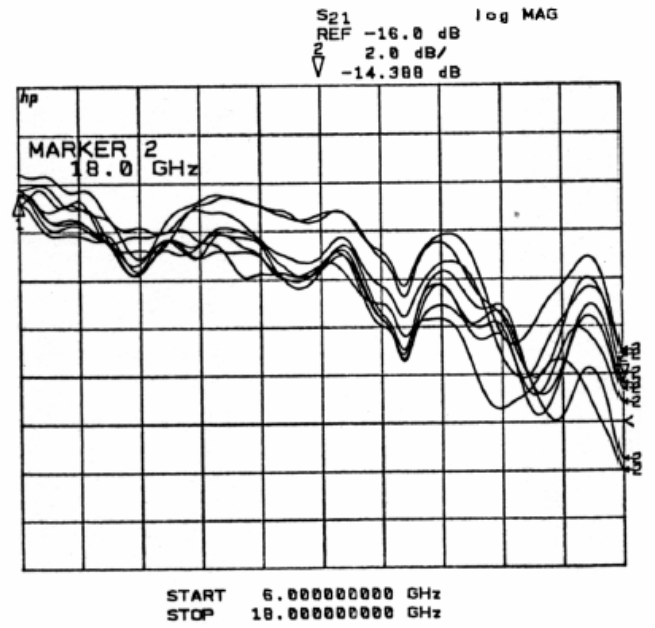


Fig. 6: Measured Insertion Loss at Major States

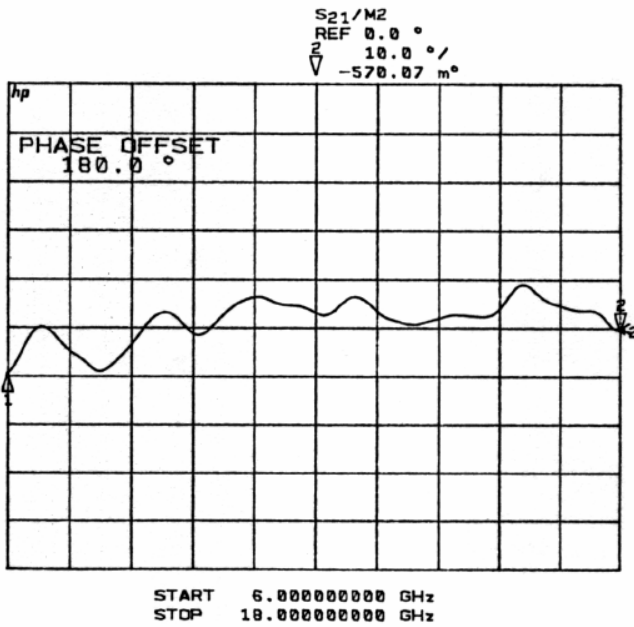


Fig. 5: Measured Phase Shift Error of The 180-deg. bit (representing the I-Q vector modulator)

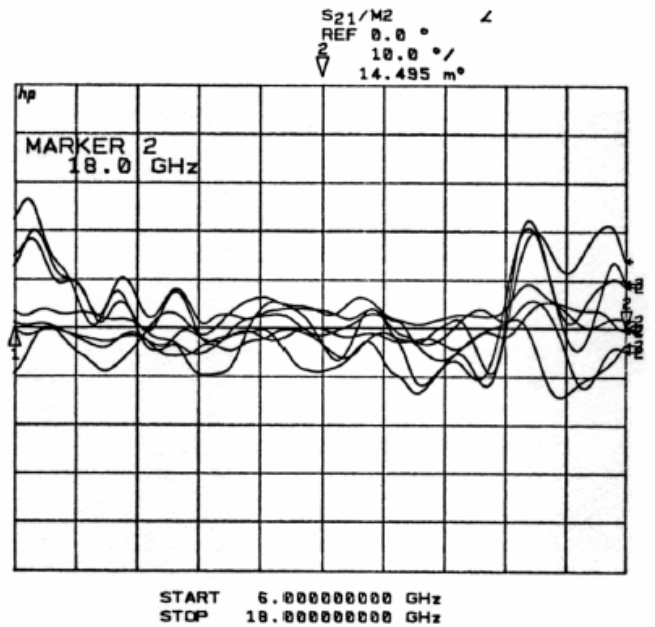


Fig. 7: Measured Phase Error at Major Phase States

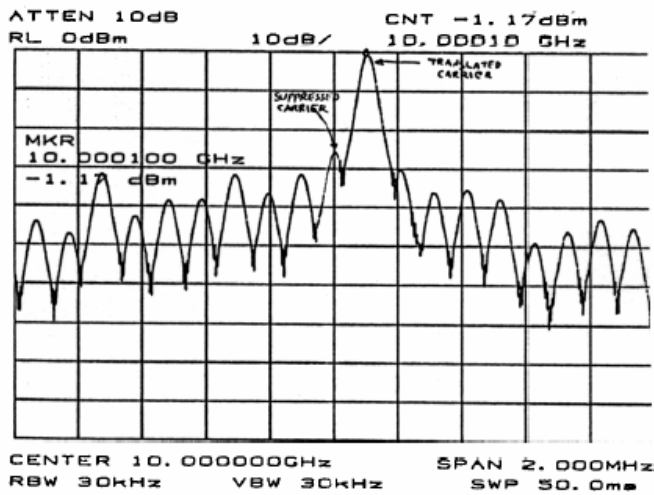


Fig. 8: Typical Translation Spectrum

#### IV. CONCLUSION

It has been demonstrated that broadband, high frequency, fast and low cost switched - bit phase shifter can be realized using ordinary MIC technology. Size and performance are comparable to MMIC design but without having to depend on a MMIC foundry and the high cost associated with that. Careful circuit layout that minimizes both leakage, coupling and radiation interaction supported with both linear circuit simulation and 3D electromagnetic simulation provide the optimum results.

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