DC to Microwave Characterization and Modeling of the Cryogenic Performance of Low-Noise HEMT's

Alina Caddemi, Francesco Catalfamo, Giovanni Crupi, Nicola Donato

Abstract – **We extensively investigated the effects of the temperature on the DC behaviour, the small signal and the noise performance at microwave frequencies of pseudomorphic HEMTs. The measured data were then employed to extract temperature dependent models by means of several extraction techniques. The relevant experimental data show that the most important electrical parameters, such as the output current, the threshold voltage, the transconductance, the forward transmission coefficient and the noise figure, are sensibly affected by thermal phenomena.**

The knowledge of the small signal equivalent circuit of microwave GaAs FET's is a crucial point for the design of low noise amplifiers and is a very useful tool to support the analysis of the transistor performance. In the present work, we report the results of our experimental activity concerning the characterization and the application of several improved procedures for the extraction of the model element values from DC, scattering (S-) parameter and noise figure measurements. The developed modeling procedures are: direct extraction, neural network techniques and evolutionary algorithm approach. The very good agreement between the simulated and measured parameters confirms the validity of the proposed methods. To carry out the experimental activity, we employed a properly designed cryogenic set-up operating in our laboratory that allows us to perform DC and microwave characterization down to 30 K.

Keywords – **Cryogenic measurement, Noise Parameters, S-Parameters, Semiconductor device modeling.**

I. INTRODUCTION

The Gallium Arsenide high electron mobility transistor (HEMT), either lattice matched or pseudomorphic (pHEMT), overcomes the performance limits of the metal semiconductor field effect transistor (MESFET) as it exhibits larger gain, higher operating frequency and lower noise figure. The carriers in the triangular (lattice matched) or square (pseudomorphic) quantum well flow in a pure crystal material and they are spatially separated from the donors by means of a spacer layer. This separation leads to a significant reduction of Coulomb scattering and carriers frozen at ionized donors under low temperature condition. Therefore the device performance improves at cryogenic temperatures as the electron mobility is enhanced by the decrease of phonon scattering processes [1, 2].

The investigation of the effects of temperature upon the performance of low-noise transistors is a key issue in designing microwave integrated circuits operating in a critical environment. In addition, knowledge of the microwave performance of high electron mobility transistors at cryogenic temperatures is of fundamental importance for the optimization of cooled radio astronomy low-noise receivers or nuclear instrumentation front-ends.

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The purpose of the present work is to report on the characterization and modeling of pseudomorphic high electron mobility transistors (pHEMT) down to 30 K.

The following of this work is organized into six Sections:

In section II we describe the device under test and the cryogenic set-up. The analyzed transistor is a commercial low noise pHEMT. The DC and RF characterization have been performed down to 30 K by a cryogenic set-up operating in our lab. A fully automated tool implemented in Agilent VEE language allows a fast, accurate and complete device characterization with a user friendly interface and software utilities for data post-processing.

In Section III we analyze the experimental results. We believe that trapping mechanisms are responsible of the kink effect, the threshold voltage shift, the reduction of the transconductance and the magnitude of S_{21} and the experimental data support our hypothesis quite reasonably.

In Section IV we describe the direct extraction method. This procedure requires only a single S-parameter measurement performed on a strong pinched-off cold FET (a zero drain source voltage Vds and a gate source voltage V_{GS} much lower than the pinch-off voltage V_{PO}) to determine parasitic ECP's [3-5]. This method does not require application of a forward bias to the gate as proposed in [6], thus avoiding device degradation due to a large gate current. The knowledge of the parasitic elements allows to extract the intrinsic elements after simple matrix manipulations to remove the parasitic effects from the scattering (S-) parameter measurement performed under "hot" bias condition ($V_{DS} > 0$ V, i.e. active device).

In Section V we report on the development of two distinct ANN-based techniques for the modeling of microwave active devices. In particular, we selected a suitable neural structure and trained it adequately to obtain a global ANN that would allow us to perform a DC and RF modeling of the DUT.

In Section VI we refer about the implementation of an Evolution Algorithm (EA) for the cryogenic noise modeling of microwave devices.

II. DC AND MICROWAVE SET-UP

As far as the cryogenic characterization is concerned, we examined a short-lead packaged pseudomorphic

(AlGaAs/InGaAs/GaAs) HEMT (Mitsubishi MGF4919G). The MGF4919 is a super low-noise transistor designed for use in L to Ku band amplifiers with a low noise figure and a high associated gain (less than 0.5 dB and higher than 12 dB, respectively, @ V_{DS} = 2 V, I_D = 10 mA and f = 12 GHz).

S-parameters of the transistor have been measured up to 6 GHz with a vector network analyser (Agilent Technologies, mod. 8753E). The devices have been placed within an air coaxial transistor test fixture (Maury Microwave, mod. MT950G) shown in Fig.1. The effects of the TTF on the measured data were properly modeled and the transistor data deembedded at the package reference planes.

Fig. 1. Photograph of the transistor test fixture (Maury Microwave TTF mod. MT950G) mounted on the thermal chuck

A full-two-port calibration of the Vector Network Analyzer (Agilent VNA mod. 8753E) is done to 7 mm references plane by using the Short-Open-Load-Thru (SOLT) method. In addition, we determine the element values of the circuit model for the TTF (see Fig. 2) [7] from S-parameter measurements of check devices (Maury Microwave mod. MT953G) at the working temperature condition by means of an optimization approach combined with an off-line calibration procedure.

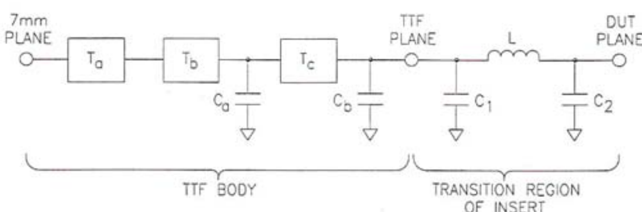


Fig.2. Circuit model of the TTF body and the insert transition region.

This model takes into account the effects of the TTF body and the insert transition region, for deembedding data at the package reference planes by means of the following relation:

$$[T_{DUT}] = [T_{TTF_LEFT}]^{-1} [T_{DUT+TTF}] \, [T_{TTF_RIGHT}]^{-1} \qquad (1)$$

where T_{DUT}, $T_{DUT+TTF}$, T_{TTF_LEFT} and T_{TTF_RIGHT} represent the transmission matrices corresponding to the scattering matrices of the device under test, the device including the effects of the TTF, the left and right parts of the TTF, respectively. To illustrate the very strong phase shift of S-parameters introduced by the TTF we report the measured forward transmission coefficient S21 with and without deembedding (see Fig. 3). In the same plot we reported also the behavior of S_{21} deembedded by using the TTF model determined at 290 K and it can be observed that neglecting the thermal dependence of the TTF leads to an increase of the phase shift at lower temperature.

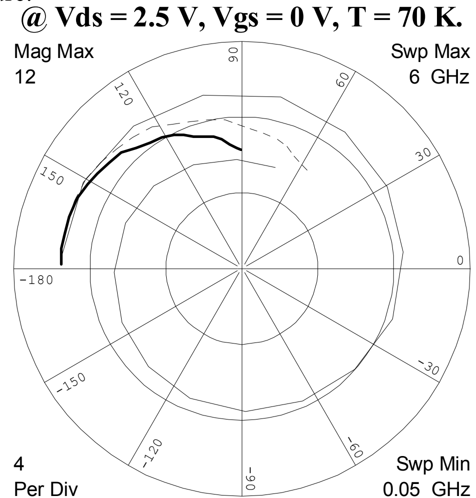


Fig. 3. Behavior of S_{21} vs. frequency at 70 K deembedded by using the model of the TTF at 290 K (dashed line) and 70 K (thick line), and without any deembedding (thin line). The bias point is V_{DS} = 2.5 V and V_{GS} = 0 V.

The TTF is placed on a liquid-helium (closed cycle) cooled metallic finger inside a vacuum chamber having microwaves coaxial feedthroughs (0 – 40 GHz) for the external instrumentation. This cryogenic set-up was designed and custom-built to perform DC and microwave characterization of devices and circuits down to 30 K. The desired temperature condition is obtained by means of a PID control loop.

The DC and RF measurements are fully automated by means of a home-made software implemented in Agilent VEE language. All operating conditions are settled and monitored by this software with an user friendly interface. The high level of automation allows to perform an accurate, fast and complete device characterization under several temperature conditions with high accuracy and great time saving.

III. EXPERIMENTAL RESULTS

A. DC characteristics

In Fig.4 we report I_D and g_{ds} vs. V_{DS} of the pHEMT measured at room temperature. A kink effect is clearly visible and V_{kink}, i.e. the value of V_{DS} at which I_D shows a sudden rise, is approximately 1.5 V. We ruled out the occurrence of an impact ionisation process since the input characteristic I_G - V_{GS} did not show the typical "bell" shape at the kink bias conditions. Over the entire investigated bias range, the gate current exhibited fairly low values (tens of nanoamps) and a

monotonic smooth dependence on either V_{GS} and V_{DS} . The trap model allows us to explain the origin of the soft breakdown in the device under test.

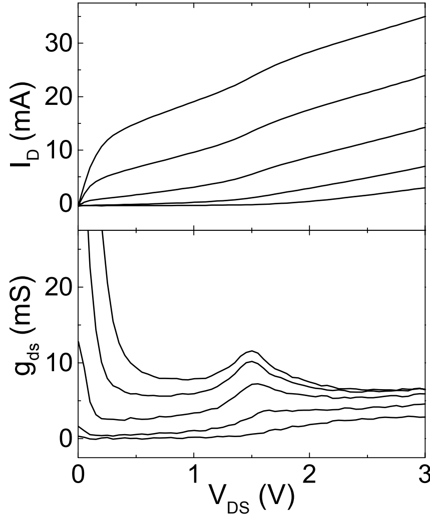


Fig. 4. Performances of I_D and g_{ds} vs. V_{DS} of the pHEMT measured at T = 295 K. V_{GS} is varied from 0 V to –0.4 V by step –0.1 V.

By increasing V_{DS}, hot electrons of the two dimensional electron gas (2-DEG) gain enough kinetic energy from the accelerating electric field in the channel to surmount the AlGaAs/InGaAs energy barrier and get then captured by donor related deep traps. As V_{DS} is increased enough, approximately to V_{kink}, the carriers trapped in the high field gate-to-drain region are released. The decrease of negative charge lowers the potential barrier, which controls the number of carriers crossing the channel, and consequently leads to a sudden rise in I_D. The size of the kink effect increases at higher V_{GS} (less negative) as the gate to drain potential barrier is lowered and thus the trapping and subsequent detrapping mechanisms are enhanced.

In Fig. 5 we show g_{kink}, i.e. the values of g_{ds} (V_{kink}), as a function of the temperature (from 295 K to 30 K). By cooling the device down to 150 K, the value of g_{kink} increases and this behavior can be explained by analyzing the output characteristics reported in Fig. 6.

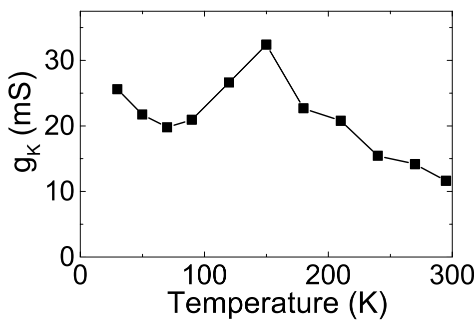


Fig.5. Performances of g_{ds} (V_{kink}) as a function of the temperature (from 295 K down to 30 K).

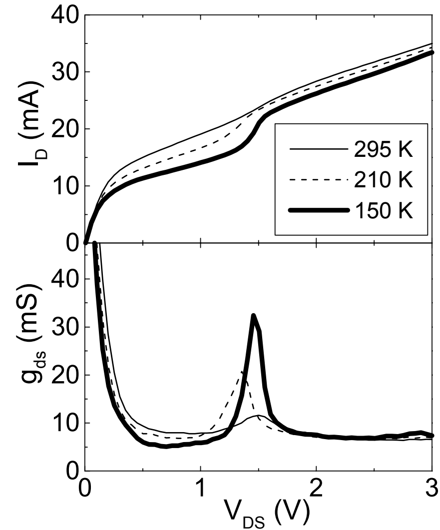


Fig.6. Performances of I_D and g_{ds} vs. V_{DS} of the pHEMT measured at V_{GS} = 0 V under three different temperature conditions (295 K, 210 K and 150 K).

It is clearly visible a reduction of I_D and an enhancement of the kink effect when the temperature decreases. As the velocity of the carriers in the undoped channel increases, due to a decrease of the phonon scattering processes, then the reduction in I_D must be caused by a decrease of the 2-DEG concentration. By lowering the temperature, only a little part of traps release carriers by thermal emission process and therefore the number of electrons in the channel decreases and the negatively charged traps further reduce the current in the channel. When V_{DS} becomes equal to V_{kink}, the filled traps release their electrons and thus the size of the kink effect increases at lower temperatures. By cooling the device from 120 K down to 30 K, I_D does not exhibit any *I-V* collapse phenomenon as shown in Fig. 7 [8, 10].

In this range of temperature, the trapping mechanisms no longer have a stronger impact on I_D than the saturation velocity enhancement. The absence of the collapse phenomenon in our device can be attributed to a reduced trap concentration in the AlGaAs layer, likely due to a lower Al mole fraction, and a better electrons confinement in the InGaAs channel.

In Fig. 8 we report I_D as a function of V_{DS} and temperature at V_{GS} = –0.3 V. By decreasing the temperature, I_D monotonically decreases because the threshold voltage shifts towards higher values. We believe that this threshold voltage shift is due to a decrease of the thermally activated electron detrapping mechanisms and the subsequent reduction of the net positive charge within the donor layer.

We extracted the threshold voltage (V_{TH}) of the device biased in the saturation region by finding the V_{GS} axis intercept of the tangent to the $I_D^{0.5}$ (V_{GS}) curve at its maximum slope point. Then the V_{TH} may be expressed as:

$$V_{TH} = V_{GSMAX} - \frac{I_D^{0.5}\left(V_{GSMAX}\right)}{\left(\frac{dI_D^{0.5}}{dV_{GS}}\right)_{MAX}} \quad (2)$$

where $\left(\frac{dI_D^{0.5}}{dV_{GS}}\right)_{MAX}$ and V_{GSMAX} are the maximum slope of $I_D^{0.5}$ (V_{GS}) curve and the corresponding V_{GS}.

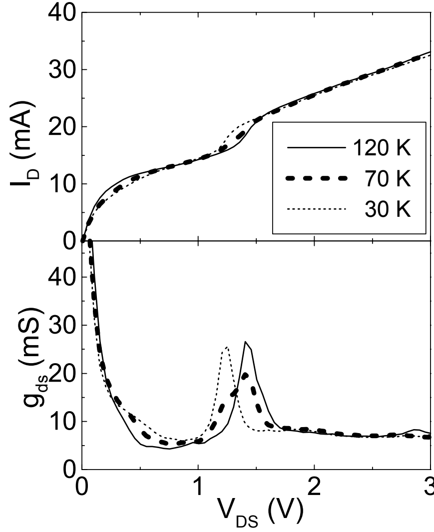


Fig. 7. Performances of I_D and g_{ds} vs. V_{DS} of the pHEMT measured at V_{GS} = 0 V under three different temperature conditions (120 K, 70 K and 30 K).

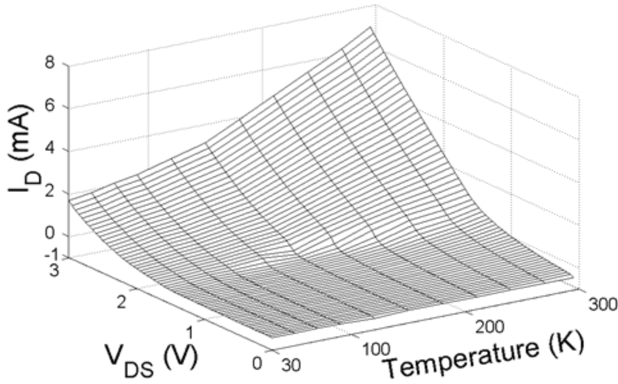


Fig.8. Performances of I_D vs. V_{DS} and temperature of the pHEMT measured at V_{GS} = -0.3 V.

At V_{DS} = 2 V and T = 295 K, the values of V_{TH} and I_D (V_{TH}) are, respectively, –0.431 V and 96.65 μA. By cooling the device down to 30 K, V_{TH} increases and V_{GS} (I_D = 96.65 μA) becomes equal to –0.288 V.

The shift of the threshold voltage leads to a degradation of g_m, which is expected to improve when the temperature is lowered as the electron mobility increases in the undoped channel. In Fig. 9 we report g_m vs. temperature and gate bias.

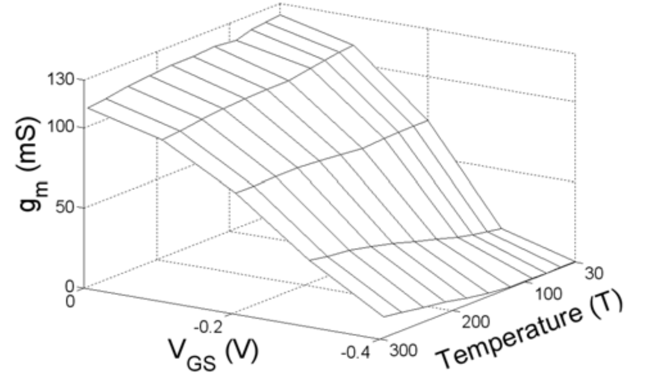


Fig.9. Behavior of g_m as a function of the temperature and gate bias at V_{DS} = 2 V.

By cooling the device, g_m increases when V_{GS} is far from the pinch-off while decreases when V_{GS} is towards the pinch off. This behavior can be explained by linking the transconductance with both the transport properties improvement and the threshold voltage shift. Near the pinch off, the threshold voltage shift has a stronger impact on g_m than the electron velocity enhancement. The influence of the threshold voltage shift on the g_m can be compensated by the bias circuitry if the device is biased by imposing I_D rather than V_{GS}.

B. RF characteristics

It is well known that the kink effect is a low frequency phenomenon since it does not occur at high frequencies [11, 12]. We calculated g_{dsRF} at low frequencies from S_{22} measurements as follows:

$$g_{dsRF} = \frac{1-\mathrm{Re}\{S_{22}\}}{1+\mathrm{Re}\{S_{22}\}} \cdot \frac{1}{Z_0} \tag{3}$$

The value of g_{dsRF} decreases when the real part of the output reflection coefficient increases as the derivative of g_{dsRF} with respect to Re $\{S_{22}\}$ is negative:

$$\frac{\partial g_{dsRF}}{\partial \mathrm{Re}\{S_{22}\}} = \frac{-2}{\left(1+\mathrm{Re}\{S_{22}\}\right)^2 \cdot Z_0} \tag{4}$$

In the device under test the real part of S_{22} increases monotonically with the increasing of V_{DS}. The real part of S_{22} and, consequently, g_{dsRF} exhibits no dispersion in the analyzed frequency range (100 KHz - 50 MHz). We evaluated the high frequency output characteristics by integrating the g_{dsRF} with respect to V_{DS}. The comparison between I_{DDC}, g_{dsDC} and I_{DRF}, g_{dsRF} is shown in Fig. 10.

The calculated values of I_{DRF} are higher than the measured values of I_{DDC} and there is not any sudden rise in the values of I_{DRF}. This behavior, which can be explained satisfactorily by the trap model, confirms that the kink effect observed in our device is due to trapping and subsequent field assisted carrier detrapping mechanisms. It is well known that trapping and

detrapping mechanisms are non equilibrium processes and the time constants of the traps are very long with respect to the reciprocal of microwave frequencies. Therefore the trapping mechanisms are low frequency physical phenomena as at high frequencies the traps cannot follow the applied signal. When V_{DS} is raised enough to allow electrons of the 2DEG to overcome the potential barrier at the AlGaAs/InGaAs heterointerface, I_{DDC} begin to be smaller than I_{DRF}. As V_{DS} becomes equal to V_{kink}, field assisted carrier detrapping phenomena at the drain side of the gate cause the kink effect.

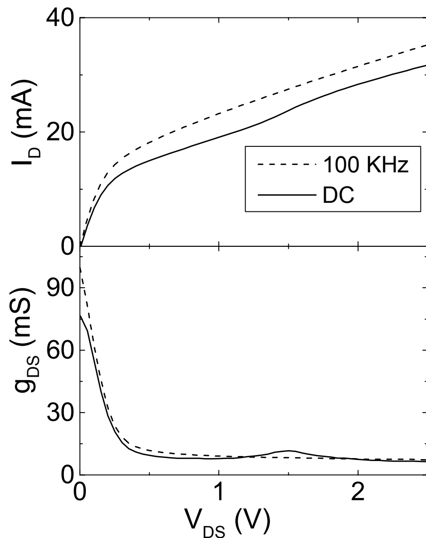


Fig. 10. Comparison between I_{DDC}, g_{dsDC} and I_{DRF}, g_{dsRF} as functions of V_{DS} of the pHEMT measured at V_{GS} = 0 V and T = 295 K. V_{DS} is varied from 0 V to 2.5 V by step 50 mV.

Although the time constants of the traps are very long, the trapping mechanisms can affect RF performances as they influences the DC quiescent bias point. By lowering the temperature, the reduction of the net positive charge under the gate due to the reduction of the detrapping mechanisms, causes a shift of the bias point resulting in a degradation of the RF performance.

The shift of the threshold voltage results turns into a decrease of $|S_{21}|$ and, consequently, in a degradation of the high frequency figures of merit, i.e. the current gain (h_{21}) and the power gain (MSG and MAG), causing a reduction of the cut off frequency (f_t) and the maximum oscillation frequency (f_{max}).

The behavior of $|S_{21}|$ as a function of the frequency and the gate bias at two different temperature conditions (290 K and 30 K) is reported in Fig. 11.

By lowering the temperature, the magnitude of S_{21} increases when V_{GS} is far from the pinch-off while decreases when V_{GS} is near the pinch off. This behavior was expected as the forward transmission parameter is strictly linked with the transconductance (see Fig. 9). The forward transmission parameter is the small signal RF gain of the transistor with its input and output matched and at low frequencies it can be defined as follows:

$$S_{21} = -2 g_{mRF} \left(R_{ds} // Z_0 \right) \tag{5}$$

RF degradation related to trapping mechanisms can be avoided if the RF small signal is applied to the transistor under pulsed bias condition [13].

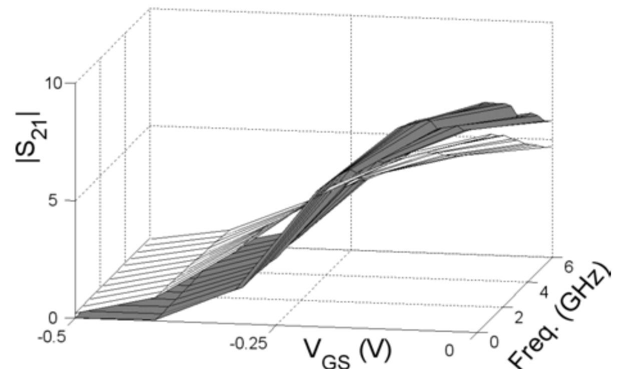


Fig. 11. Magnitude of S_{21} as a function of frequency and gate bias at the temperature of 295 K (white plot) and 30 K (gray plot) for a fixed drain bias of 2 V.

IV. DIRECT EXTRACTION PROCEDURE

As far as the equivalent circuit is concerned, it is of basic importance to choose the most appropriate model topology for the specific case considered as the values of the extracted ECP's depend on the model topology. In Fig. 12, we show the small signal equivalent circuit adopted for the tested device. The equivalent circuit is commonly partitioned into an extrinsic section, basically including bias-independent elements, and an intrinsic section with bias-dependent elements. The extrinsic elements are L_g, L_s, L_d and R_g, R_s, R_d which represent the gate, source, drain inductances and the gate, source, drain resistances, respectively. The intrinsic elements are the gate source capacitance C_{gs}, the gate source resistance R_{gs}, the transconductance g_m, the transit time delay τ, the gate drain capacitance C_{gd}, the output conductance g_{ds} and the drain source capacitance C_{ds}.

We neglected the effect of parasitic capacitances because we employed measurements performed up to 6 GHz, whereas these elements should be included in the equivalent circuit when working at higher frequencies. If the influence of the parasitic capacitances is neglected improperly, then the intrinsic capacitances will be overestimated as they will encompass the parasitic capacitance effects.

The extraction of ECP values by means of *S*-parameter measurements is an ill-conditioned problem as there are too many unknowns and not enough equations (eight equations representing the *S*-parameters expressed in terms of the ECP's at a fixed frequency). In the scientific literature several methods have been proposed [3, 14] to solve this problem and they can be classified into two categories: optimization-based [15] and direct (or analytical) extraction techniques [3-6]. However, it is well known that the optimization procedures may lead to element values with no physical meaning and the results depend either on the starting parameter values and the optimization method itself. The analytical procedures

overcome these drawbacks and allow to extract the ECP's straightforwardly.

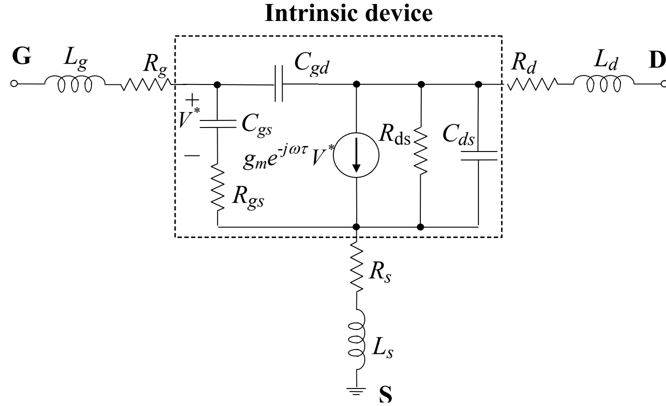


Fig.12. Equivalent circuit adopted for the device under test. The intrinsic elements are shown in the dashed box.

By these direct methods, the parasitic ECP's are extracted from S-parameter measurements performed at "cold" bias (V_{DS} = 0 V, i.e. passive device). Under this bias condition there are not electrons flowing from source to drain and therefore g_m is equal to zero. Two equations vanish ($S_{12} = S_{21}$) as the transistor becomes reciprocal but, at the same time, the two unknowns g_m and τ disappear [16]. Moreover, the gate-source and gate-drain intrinsic circuits can be assumed equal. Although the validity of this approximation depends on the transistor lay-out structure, it is conventionally assumed that the intrinsic device structure is highly symmetric due to the symmetry of the depletion region under the gate at V_{DS} = 0 V. Therefore, the relevant circuit analysis becomes much easier under "cold" condition since the intrinsic circuit can be simplified. The several "cold" methods reported in the literature differ for the value of V_{GS} employed. We adopt a procedure which requires only a single S-parameter measurement performed on a strong pinched-off cold FET (V_{DS} = 0 V, $V_{GS} \ll V_{PO}$) to derive parasitic ECP's. The knowledge of the parasitic elements allows extracting the intrinsic elements after simple matrix manipulations required to remove the parasitic effects from the S-parameter measurements performed under "hot" bias condition (V_{DS} > 0 V, i.e. active device).

At strong pinch-off bias, the channel is completely depleted and therefore the capacitances C_{gs}, C_{gd} and C_{ds} become the dominant intrinsic circuit elements (see Fig. 12). In order to simplify the circuit analysis the capacitive ∏ network is transformed into the corresponding T network consisting of the capacitances C_g, C_s and C_d [15]:

$$C_g = C_{gs} + C_{gd} + \frac{C_{gs} C_{gd}}{C_{ds}} \tag{6}$$

$$C_s = C_{gs} + C_{ds} + \frac{C_{gs} C_{ds}}{C_{gd}} \tag{7}$$

$$C_d = C_{ds} + C_{gd} + \frac{C_{ds} C_{gd}}{C_{gs}} \tag{8}$$

It can be noted that we do not need to assume that the gate-source and gate-drain intrinsic circuits are equal, which would imply $C_{gs} = C_{gd}$.

Then, the Z-parameters of the strong pinched-off device are [3-5]:

$$Z_{11} = R_s + R_g + j\left[\omega\left(L_s + L_g\right) - \frac{1}{\omega}\left(\frac{1}{C_g} + \frac{1}{C_s}\right)\right] \tag{9}$$

$$Z_{12} = Z_{21} = R_s + j\left[\omega L_s - \frac{1}{\omega C_s}\right] \tag{10}$$

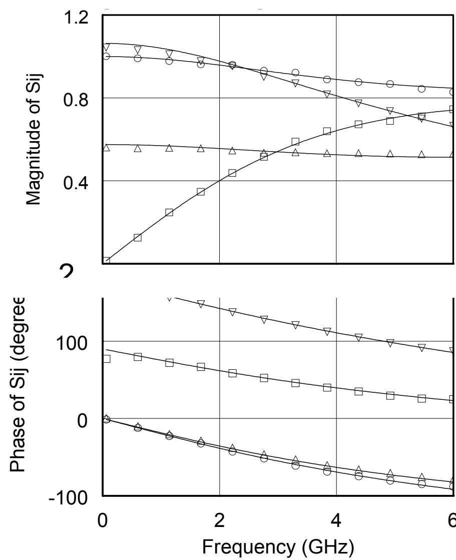
$$Z_{22} = R_d + R_s + j\left[\omega\left(L_s + L_d\right) - \frac{1}{\omega}\left(\frac{1}{C_s} + \frac{1}{C_d}\right)\right] \tag{11}$$

The parasitic inductances are extracted from the slopes of straight lines interpolating the experimental data of the imaginary parts of the Z-parameters multiplied by the angular frequency ω, vs. ω^2. These lines are defined by a least square regression. The parasitic resistances are obtained by averaging the real parts of Z-parameters. The S-parameters measured under "hot" condition are converted to Z-parameters and the six extrinsic elements are subtracted [3]. The resulting Z-parameters are then converted into Y-parameter since the intrinsic circuit is based on a ∏ topology. Finally, the seven intrinsic elements are computed by averaging the values analytically extracted at each frequency point from intrinsic Y-parameters according to the expression proposed in [14].

The method employed is very fast as it needs only two S-parameter measurements and moreover the characterization and modeling procedures are completely automated by means of a user friendly home-made software developed with Agilent VEE tools. By employing this modeling procedure, we extract ECP values that allow accurate device simulation without any tuning or optimization steps. The good agreement between measured and modeled S-parameters have been found at all investigated bias and temperature conditions and that confirms the validity of the employed procedure.

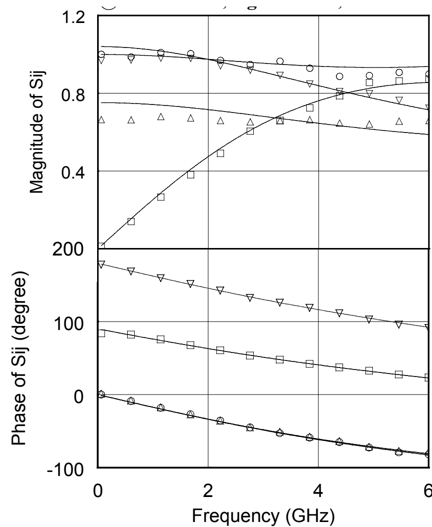
As an example, in Fig. 13 we report the comparison between measured and modeled S_{ij} parameters and the relevant percentage errors E_{ij} at V_{DS} = 1.8 V and V_{GS} = –0.2 V under two different temperature conditions (290 K and 30 K).Under this bias condition, cooling the device from 290 K down to 30 K leads to small variations of the S-parameters such as the phase shift of the input reflection coefficient S_{11} towards 0° (the phase of S_{11} measured at 6 GHz increases from 88.1° to 81.8°) due to the observed lower C_{gs} and the increase of the magnitude of the reverse transmission coefficient S_{12} ($|S_{12}|$ measured at 6 GHz rises from 0.074 to 0.087). It is interesting to note that it does not affect significantly the magnitude of S_{21} which represents a small signal RF gain factor of the device. Since this scattering parameter is strongly correlated to g_m (see Fig. 9), its behavior at lower temperature can be linked to the counterbalancing of the electron transport properties improvement and the

decrease of the 2DEG concentration linked to the V_{TH} shift. As a consequence, by lowering the temperature down to 30 K $|S_{21}|$ rises only when V_{GS} is far from the pinch-off condition (see Fig. 11).



(a)

E_{11} = 1.6%, E_{12} = 2.8%, E_{21} = 1.8%, E_{22} = 2.2%.



(b)

E_{11} = 3.7%, E_{12} = 5.1%, E_{21} = 3.1%, E_{22} = 7.2%.

Fig.13. Comparison between measured (symbols) and modeled (solid lines) S_{ij}-parameters with the relevant percentage errors E_{ij} over a frequency range extending from 60 MHz to 6 GHz. The working condition is V_{DS} = 1.8 V, V_{GS} = -0.2 V and the temperature equal to 290 K (a) and 30 K (b). S_{11} (circles), S_{22} (up triangles), 10*S_{12} (squares) and S_{21} /5 (down triangles).

V. Neural Network Techniques

In this section we report the development of two distinct ANN-based techniques for the modelization of microwave active devices. In particular, we selected a suitable neural structure and trained it adequately to obtain a global ANN that would allow us to perform a DC and RF modeling of the DUT. Furthermore, an ANN software utility for the noise characterization of microwave transistors down to cryogenic temperatures is reported. By this last procedure, jointly with an original characterization software written in our lab, we are able to reproduce the noise performance of several device types from only one measured S-parameter set, one frequency point and one noise figure (namely, F_{50}) value.

The adopted structure for the basic neural network arrangement is the so-called Multi-Layer Perceptrons (MLPs) with three stages (input and output layers and only one layer of hidden neurons). It has to be noted that MLP networks trained with a back-propagation algorithm are able to perform a general nolinear input/output mapping from the input space to the output space. The capability of opportunely trained MLP structures to approximate arbitrary continuous functions has been established by the so-called Cybenko theorem [17]. To this aim, the Levenberg-Marquardt (LM) back-propagation algorithm allows a reasonably good training of the ANNs structure. As a matter of fact, the LM algorithm has been tested on several function approximation problems and the obtained results indicated that it is very efficient when training networks having up to a few hundred weights [18].

An other aspect not to be underestimated is the MLP sizing. Indeed, the determination of the number of units to be employed in the hidden layer is not usually as straightforward as it is for the input and output layers. It has been established that a MLP with a number of neurons in the hidden layer too low cannot converge at all, while an oversized one can reach a very good error index, but it cannot perform a good global performance due to the excessive number of involved variables. In the scientific literature, a monitoring approach aimed at finding the optimal neuron number by cutting out the neurons that less contribute to the network behavior has been reported [19]. In addition, the use of a genetic algorithm approach to address the issue of the optimal topology of a MLP structure has been also presented [20].

Taking into account all the previous considerations, we firstly determined the ANN shown in Fig. 14, that was obtained by assembling three different subnets. The first subnet has three inputs and only one output. These inputs correspond to the values of the gate and drain voltages V_{GS},V_{DS} and the operating temperature T. The output gives the value of the drain current I_{DS} of the DUT. By suitably training this neural network, we could reproduce the DC behavior of the DUT, namely I_{DS} = f(V_{DS} ,V_{GS}). In order to build up a suitable training set for the neural network, we have employed cryogenic DC and microwave measurements of a pHEMT device (MGF4319 by Mitsubishi Semiconductors) previously performed in our lab. The characterization data for this transistor were taken over a wide range of operating temperatures (from 220 K to 70 K) and in 0.05–6 GHz

frequency range. Indeed, the measurements span the following ranges of parameter variability:

$0 \le V_{DS} \le 2.5$ V; $0 \le |V_{GS}| \le 0.6$ V; $0 \le I_{DS} \le 31.6$ mA.

The second and the third networks have the same four inputs, namely V_{DS} ,V_{GS}, T and the frequency *Freq*, and present as outputs the magnitude and the angle of the S-parameters, respectively. By these two subnets we model the small-signal behavior of the DUT.

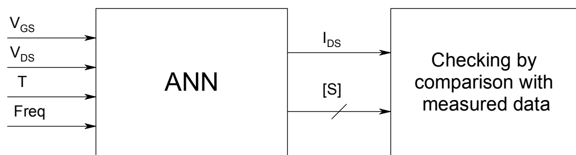


Fig. 14. Block diagram of the procedure for the I-V curve and S-parameter extraction.

By carrying out a suitable training step for all the subnets, the performance of the ANN structure is thus checked by comparison with a set of measured data that are not included in the training data set. In Fig. 15 we report the I-V curve comparison between test data and measured data for an operating temperature of 70 K. An analysis of this plot shows that the first subnet reproduces with a very good agreement the behavior of drain current I_{DS} vs. V_{GS} and V_{DS} voltages at the chosen temperature.

An ANN software utility for the determination of the noise parameters (NP) of the DUT are also developed, and the NP's thus obtained are compared with direct measured experimental data. A cryogenic temperature test is also performed leading to very good results. It can be seen that the difference occurring between the expected NP values and the values calculated by the neural network does not evidence significant variations in the behavior of extracted noise parameters.

By this ANN-based procedure, we are thus able to simulate the HEMT noise parameters of several device types from a reduced data set. The employed noise figure is that measured in input matched conditions, namely F_{50}.

The trained network outputs were compared with data of available noise measurements and the results were in very good agreement with the available data. It can be observed that the difference occurring between the expected value of the NPs and the value calculated by the neural network is negligible.

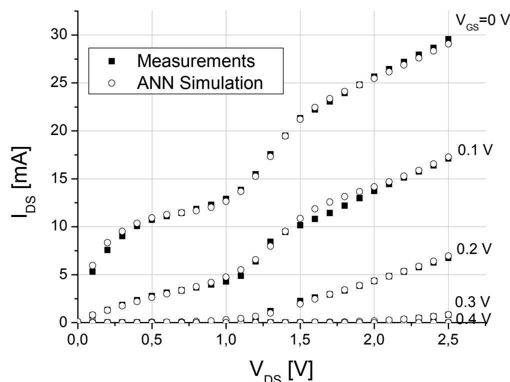


Fig. 15. I-V curve comparison between test data and measured data @ T = 70 K.

Fig. 16 reports the adopted MLP structure of the developed ANN, that is composed of three layers. The input layer consists of ten neurons and its inputs are the scattering parameters S_{11}, S_{12}, S_{21}, S_{22} (magnitude and phase), one frequency value and one noise figure value (i.e. F_{50}). The output layer consists of four neurons, each corresponding to the four noise parameters of the DUT. Finally, the hidden-layer employs twenty seven neurons.

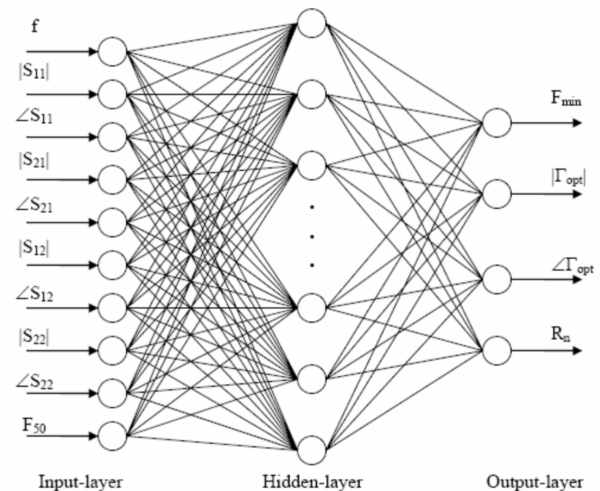


Fig. 16. The three-layers MLP structure adopted for ANN.

By adopting this procedure, the ANN was initially trained by using data available from performed measurements. More specifically, it has employed the following devices (super low-noise pHEMT):

i. Mitsubishi: MGF4319 (vs temperature);
ii. NEC: NE20283 (vs temperature and bias);
iii. Celeritek CF001 (vs temperature).

Note that for the Mitsubishi device the measurements have been performed down to cryogenic temperatures, in the 6–18 GHz frequency range. In the training set, it were used data available for all devices except those concerning the MGF4319 device at 65 K and 115 K. These data, together with other data, were employed for the validation set. The training time strongly depends on computer hardware characteristics. However this time is quite shorter than the tuning time required in CAD modeling procedures. Several ANN implementations with different numbers of hidden neurons were used for training step. By means of a performance analysis we were able to choose the best ANN model with the right balance between training time and output error.

The neural network was tested with cryogenic temperature measurements of the MGF4319 device. The characterization data for this transistor were taken at different values of operating temperatures down to cryogenics levels (from 290 K to 65 K). In Figs. 17-19 it is shown the performance of the neural network in terms of the NP's for MGF4319 at 65 K and 115 K.

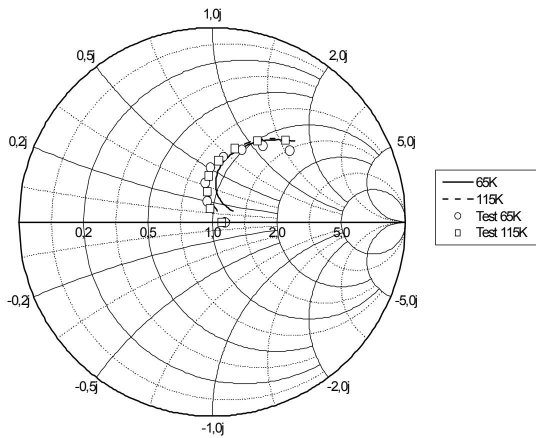


Fig. 17. MGF4319 testing: comparison between test data and measured data for the optimum noise source reflection coefficient vs. temperature, in the 6 – 18 GHz frequency range.

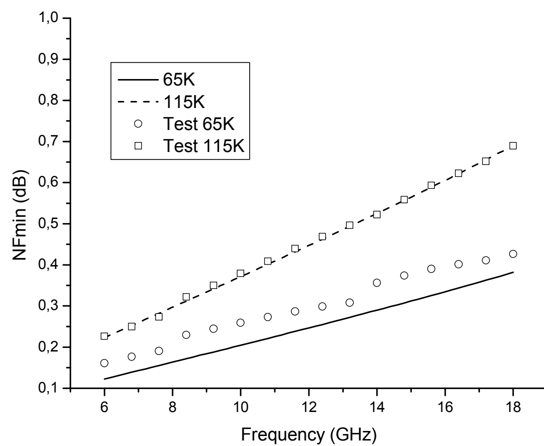


Fig. 18. MGF4319 testing: comparison between test data and measured data for the minimum noise figure vs. temperature.

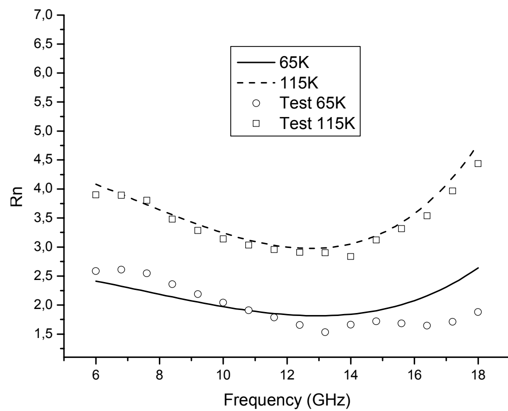


Fig. 19. MGF4319 testing: comparison between test data and measured data for the noise resistance, vs. temperature.

A careful analysis of these diagrams allows to verify that the neural network generates a reasonably good prediction of the NP values down to cryogenic temperatures. It is here reported the behaviour of the minimum of noise figure and the noise resistance vs. frequency and temperature for all data generated by ANN procedure. More specifically, in Fig. 20 it can be seen that the minimum noise figure increases when the frequency increases and decreases when temperature decreases, as expected. In Fig. 21 it can be seen how the behaviour of the noise resistance is a parabolic-like type vs. frequency and, for a specified frequency, its value increases with temperature.

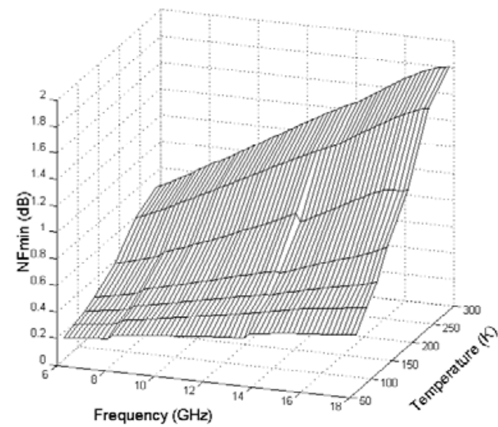


Fig. 20. Minimum noise figure vs. frequency and temperature.

The U-shaped behaviour vs. frequency is due to the parasitic effects (inductance-type) in the DUT. For the intrinsic device, the noise resistance is almost independent from frequency over the entire microwave range. Moreover, the performance of R_n strongly depends on the device characteristics. The role played by the input bonding inductance causes a marked decrease of the values of R_n offered by up-to-date chip devices, though introducing a frequency dependence.

By improving the device characteristics with better materials and well-confined 2-D electron gas in the undoped channel, very low frequency independent values of R_n are expected from the chip device, thus making the inductance influence less acceptable [21].

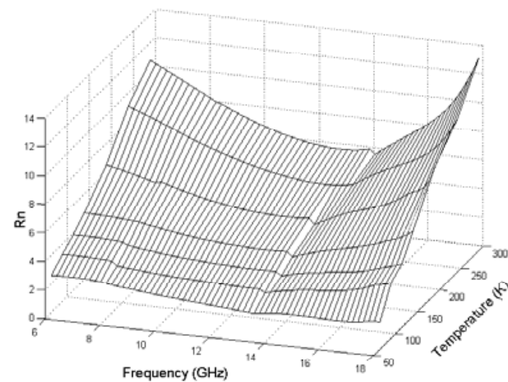


Fig. 21. Noise resistance vs. frequency and temperature.

Finally, it can be seen that the minimum noise figure F_{min} and the noise resistance R_n are sensibly affected by thermal variations, whereas the optimum noise reflection coefficient Γ_{opt} is not. Upon decreasing the lattice temperature, the noise parameters F_{min} and R_n lower because the temperature variations of the high-field electron velocity cause an increase of the transconductance. In addition, lower operating

temperatures cause the decrease of the thermal noise and the reduction of the diffusion noise, which is the dominant noise in field-effect devices at microwave frequencies [22].

VI. EVOLUTIONARY ALGORITHM APPROACH

We here refer about the implementation of an Evolution Algorithm (EA) for the cryogenic noise modeling of microwave devices. Some preliminary applications of the EAs in the field of microwave component simulations have recently appeared in the scientific literature [23, 24], but here we have shown how EA's can be employed to solve the noise modeling problem according to a black-box approach. The application refers to the simulation of the NPs of HEMT in the 6-18 GHz frequency range and down to cryogenic temperatures (90 K) compared with experimental data. The quality of results indicates that EA techniques represent a truly alternative way to determine the microwave noise performance of HEMT devices, thus furnishing a flexible tool to support CAD of high sensitivity – ultra high speed circuits. In this case, the application of such algorithms concerns the performance of advanced microwave and millimeter-wave devices employed in the development of ultra-high bit rate telecommunication systems since the saturation of lower frequency slots and the need of wider bands pushes towards the requirements of ever increasing operating frequencies.

The evolution algorithms are adaptive procedures that are mostly used for optimization and research problems [25]. These procedures are conceptually based on the principles of the natural evolution of the species. Living organisms consist of many cells and each cell contains one or more chromosomes that can be divided in genes. Each gene codifies a specified feature of the living organism. From the point of view of the information theory, the chromosome refers to a candidate solution.

In the present analysis, a set of eight base functions constitutes the collection of the chromosomes, namely the initial population. This set realizes an infinite population of functions since the related coefficients are an infinite collection. Moreover, the main program of the EA assigns a set of suitable coefficients to the base functions. Subsequently, these functions combine with each other. The high number of the potential solutions obtained ensures the generation of an optimum solution that exhibits the lowest error compared to the maximum fixed threshold. The "fitness" is warranted by a continuous comparison between the candidate solution and the measured value of each NP. The comparison ends when a chosen threshold for the fitness is reached. A convergence procedure is also carried out to refine the generated solutions by exploring its neighbor regions. The selection is achieved by successive "mutation" steps. In Fig. 22 it is reported a flux diagram describing the adopted EA procedure.

The obtained analytical equations thus provide an estimation of the behaviour of the NP's down to cryogenic temperatures and also outside the frequency range under observation. This approach is original and very flexible because it does not require a training procedure like in the ANN-based systems. It also allows to perform an analysis of the stability performances of the parameters under test. By this procedure, a complete set of the NP's for a commercial super low-noise pseudomorphic HEMT has been obtained. This transistor was previously measured in our laboratory and a complete noise characterization was performed vs. frequency and temperature.

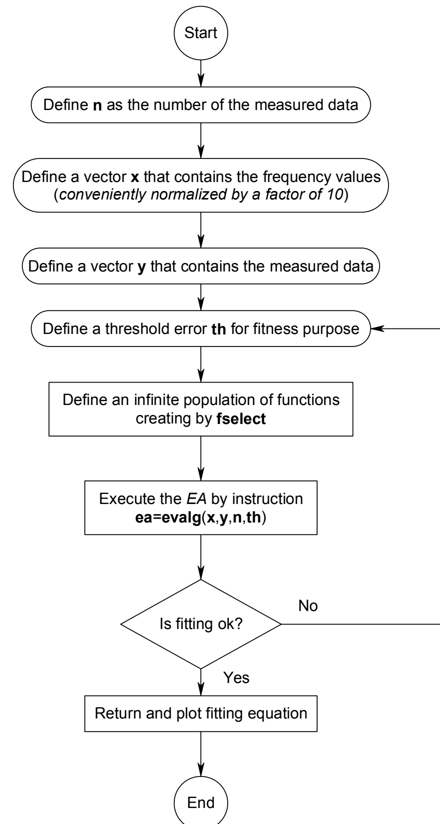


Fig. 22. Flux diagram of the adopted EA procedure.

Therefore, the EA performance for the noise modeling of the DUT has been checked by using these experimental data in the 6-18 GHz frequency range and down to cryogenic temperatures. The comparison between measured data and EA simulation of the NP's vs. frequency and temperature (290-90 K, step 50 K) for the chosen DUT was performed and the results are reported in Figs. 23–25.

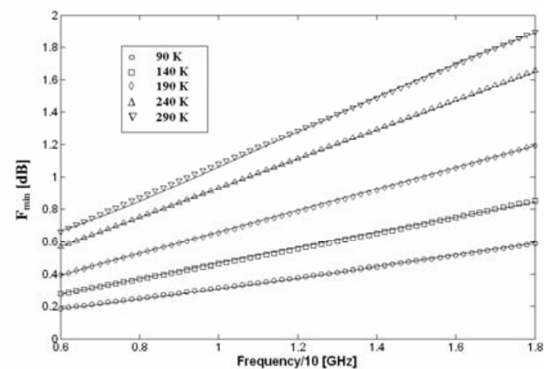


Fig. 23. Comparison between experimental data and EA simulation of the minimum noise figure F_{min} vs. frequency and temperature for the MGF4319 device.

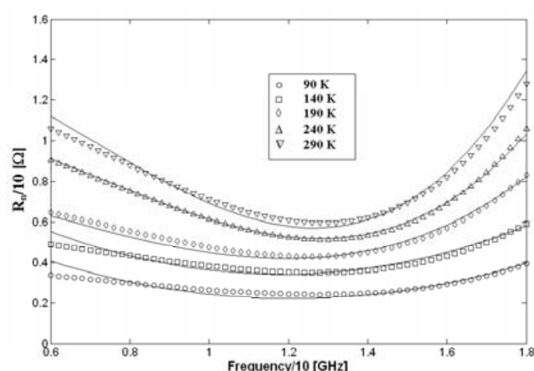


Fig. 24. Comparison between experimental data and EA simulation of the noise resistance R_n vs. frequency and temperature for the MGF4319 device.

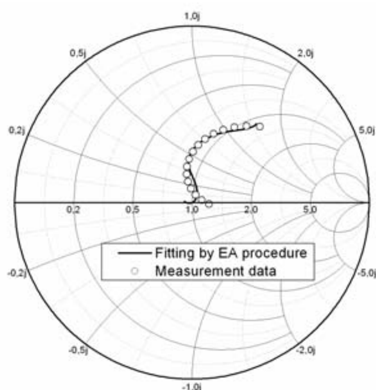


Fig. 25. Comparison between experimental data and EA simulation of the optimum noise reflection coefficient Γ_{opt} vs. frequency for the MGF4319 device at 90 K on the Smith chart.

The following equation set (eqs. 12–14) reports the analytical expressions of the functions obtained by application of the EA procedure at all the considered temperatures (excepted for Γ_{opt}, which are reported only the functions at 90 K):

$$\begin{aligned} F_{min}\big|_{@90K} &= \exp\left(\frac{0.7351f-2.1501}{0.4636f+0.7351}\right) \\ F_{min}\big|_{@140K} &= \exp\left(\frac{1.9144f-4.0898}{1.2274f+1.5319}\right) \\ F_{min}\big|_{@190K} &= \exp\left(\frac{1.3494f-2.0587}{0.8628f+0.8093}\right) \\ F_{min}\big|_{@240K} &= \exp\left(\frac{3.513f-3.7513}{1.864f+1.8204}\right) \\ F_{min}\big|_{@290K} &= \exp\left(\frac{3.2979f-3.0679}{1.6286f+1.6006}\right) \end{aligned} \tag{12}$$

$$\begin{aligned} R_n/10\big|_{@90K} &= 0.49868f^2-1.2057f+0.95 \\ R_n/10\big|_{@140K} &= 0.62895f^2-1.48671f+1.2057 \\ R_n/10\big|_{@190K} &= 0.43994f^3-0.7293f^2-0.1469f+0.886 \\ R_n/10\big|_{@240K} &= 0.88564f^3-1.9552f^2+0.6505f+1.033 \\ R_n/10\big|_{@290K} &= 1.2225f^3-2.5875f^2+0.67398f+1.3844 \end{aligned} \tag{13}$$

$$\begin{aligned} \left|\Gamma_{opt}\right| &= -0.512365f+0.88114 \\ \angle\Gamma_{opt}/180 &= -1.4358f^3+4.0684f^2-3.3195f+1.1199 \end{aligned} \tag{14}$$

where f is the normalized frequency (by a factor of 10).

In Table 1 we show the percentage average error (PAE), calculated over the whole temperature range, obtained by using the EA functions determined.

TABLE 1
PAE USING EA FUNCTIONS

Noise Parameter	PAE
F_{min}	0.47
R_n	1.58
$\lvert\Gamma_{opt}\rvert$	2.43
$\angle\Gamma_{opt}$	3.05

Finally, a thorough analysis of these plots allows to establish that application of the EA technique produces reasonably good values of the NP's down to cryogenic temperatures for the DUT. Such results can be effectively employed either in analyzing the device performance in a wide range of operating conditions and in computer-aided design of low-noise circuits. An other advantage with respect to a concurrent black-box modeling approach, i.e. that employing ANN techniques where a critical training step must be carefully carried out, this algorithm adapts itself to whichever device performance without the need to supply any additional information.

VII. CONCLUSION

The aim of this work has been to give an overview of our most recent work in the field of characterization and modelling of advanced microwave transistors down to cryogenic temperature. Measurements of the DC characteristics, S parameters and noise figure have been investigated in detail with respect to the temperature. Furthermore, our efforts have been dedicated to extract robust models which can accurately represent the measured device characteristics over the entire analyzed temperature range. The obtained good level of agreement between measurements and models has confirmed the validity of the proposed extraction procedures, which are based on different types of approaches: analytical equations, by direct extraction, neural networks and evolutionary algorithms.

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