A Solution for Efficient Reduction of Intersymbol Interference in Digital Microwave Radio

Vladimir D. Orlic[1], Miroslav Lutovac[2]

Abstract – **In this paper we describe one simple solution for improving the performance of digital microwave radio system under conditions of intersymbol interference. Presented structure of "blind" adaptive equalizer is characterised with low complexity, suitable for implementation on FPGA, and can be used for efficient reduction of intersymbol interference in order to satisfy demands defined by standardization institutions.**

Keywords – **Adaptive equalizer, blind equalization, intersymbol interference, digital microwave radio**

I. INTRODUCTION

Intersymbol interference (ISI) caused by frequency-selective multipath propagation may be the reason of serious degradation of digital microwave radio system performance. This problem is treated in recommendations regarding design and operation of radio-relay (RR) systems ([1]-[3]). System's robustness to frequency-selective propagation conditions is commonly defined in form of M-curve signature measurements [4], performed during laboratory tests of RR devices, and calculation of system performance is done on basis of achieved results. The goal is to satisfy the limits defined in recommendations; since the influence of frequency-selective fading on microwave radio is increasing rapidly with path length and operating frequency, in many applications involving some kind of protection against frequency-selective fading is necessary in order to achieve this.

Two countermeasures to propagation distortion are commonly used: diversity techniques and adaptive channel equalizers. Since the usage of diversity within RR systems seriously increases realization and maintenance costs, adaptive equalizers are considered to be very attractive solution to combat multipath fading effects. Time domain equalization is the most natural approach, since it attacks intersymbol interference directly: during the acquisition process previously distorted signal can be processed with the goal to re-establish its original quality, commonly observed in context of signal eye-pattern. In most communication systems that employ equalizers channel characteristics are unknown a priori, and, in many cases, channel response is time-variant. In such a case, the equalizers are designed to be adjustable to the channel response and, for time-variant channels, to be adaptive to the time variations in the channel response [5].

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In addition, very often the concept of communication system itself restricts the possibility of using training sequences for equalizer structure adaptation. This means that, in numerous cases, adaptive equalizers are forced to work in so-called "blind" mode, making decisions and performing adaptation on the basis of received signal's waveform only.

Solutions present in modern RR devices differ in complexity and efficiency: ability of microwave radio in combat with multipath fading, usually described through categories of average fade depth and dispersive fade margin (DFM)[4], lay in wide spectra of values – from 25 dB to more than 40 dB in reported average notch depth values, and from 43 dB to 71 dB in values of DFM ([6]-[9]). Solutions that are being considered for superior commonly consider powerful adaptive equalizers, with large number of coefficients, wide data formats for high precision and signal processing at rates higher than symbol rate. All these facts implicate very rigorous demands in design and implementation of adaptive equalizer structures: complex structures occupy large amount of digital logic while, at the same time, the level of signal latency has to be low enough for achieving appropriate operation speed. However, solutions with relatively low complexity, carefully designed to be resource-efficient, may also satisfy limits defined in recommendations. Instead of using application-specific platforms for this purpose, it is possible to use standard reprogrammable hardware, like CPLD and FPGA chips, without any crucial loss in efficiency of intersymbol interference reduction process. In this paper we propose one solution for adaptive equalizer, characterised with simple structure and good flexibility, that guarantees appropriate performance of RR device under selective fading conditions.

II. LOW-COMPLEXITY ADAPTIVE EQUALIZER

The basic structure of adaptive equalizer that's been explored is shown in Fig. 1.

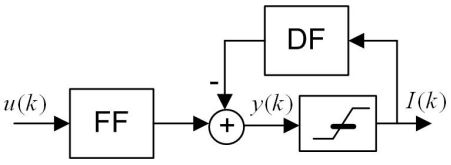

Fig. 1. Adaptive equalizer scheme.

It includes feed-forward (FF) and decision-feedback (DF) sections, realised in form of baud-spaced adaptive filters with minimum necessary number of taps. For the reasons of simplicity, LMS algorithm is chosen for adaptation of

coefficients in both of these sections; operation of adaptive equalizer presented in Fig. 1 may be expressed by following equations:

$$y(k) = \sum_{j=1}^{N} C_j u(k-j+1) - \sum_{i=1}^{M} B_i I(k-i+1) \quad (1)$$

$$C_j(k+1) = C_j(k) + \mu \cdot \varepsilon(k) \cdot u(k-j) \quad (2)$$

$$B_i(k+1) = B_i(k) + \mu \cdot \varepsilon(k) \cdot I(k-i) \quad (3)$$

$$\varepsilon(k) = I(k) - y(k) \quad (4)$$

where $u(k)$ stands for (unequalized) input signal, $y(k)$ for signal after equalization, $I(k)$ for results of comparison of $y(k)$ with threshold value, $\varepsilon(k)$ for error signal and μ for multiplication constant for weighting the adaptation of values of tap coefficients C_i (FF section) and B_i (DF section).

During previous work, we showed that FF structure with only 3 taps is good enough for achieving more than 3 dB in improvement of average value of system signature depth; at the same time, we reported that maximum speed of operation of proposed structure is practically at the limits for operation with medium-capacity RR device ([10],[11]). The presence of DF section improves the reduction of intersymbol interference regarding to previous symbols in incoming data sequence, but it also seriously increases the latency of system clock. Thus, it is necessary to explore the minimum demands in amount of logic resources for implementation that lead to fast operation of adaptive equalizer and efficient reduction of ISI, as goals with equal importance.

Signal at the input of equalizer ($u(k)$) is in form of 8-bit parallel data, coded as unsigned integer value. Its format is defined by offset AD converter used for conversion of bipolar analogue signal prior to equalization. To ensure that analogue signal is positioned at appropriate range of values, an external AGC (Automatic Gain Control) circuitry is used. AD conversion is performed at system clock rate, equal to symbol rate of incoming data sequence, and samples are taken at position of maximum eye-pattern opening. For this purpose external PLL circuit is used, based on voltage-controlled oscillator operating at symbol rate frequency and value of its phase is considered to be optimal. After entering the equalizer, input signal is first converted to signed values by reducing for value of half-scale (128), and then routed to FF section as 8-bit signed integer. Since the expected values of FF filter coefficients C_i after convergence are relatively small (around 0 and 1), results of multiplication of FF filter taps with filter coefficients, just like results of their further summation, require additional bit for achieving full range of potential values (having in mind that there are only 3 taps in FF section). Thus, results of multiplication and addition at these points of equalizer need 9-bit registers for storing signed integer values. Although coefficients C_i have fractional parts of values, that are being crucially important for system operation, during research we concluded that fractional parts of multiplication and addition results on path through FF section mentioned above can be ignored without any significant loss in precision. Ignored values are negligible in comparison with integer parts of attained values – by ignoring them serious saving in amount of digital resources is achieved. If the values of DF section output are controlled to be small enough, the final result of equalization ($y(k)$) can be described in similar manner – this was the direction of interest exactly, and $y(k)$ values are also formed at 9-bit registers as signed integers, without any fractional part. At this point decisions can be made on the basis of $y(k)$ by simple comparison with value of zero – this is direct consequence of signed nature of equalization result signal. Positive and negative samples of $y(k)$ are simply replaced with approximately full-scale signal values and this is how signal $I(k)$ is generated.

Error signal $\varepsilon(k)$ is generated from $y(k)$ and $I(k)$, according to equation (4). It's value is also stored in 9-bit register, and used in process of coefficients adaptation. Since adaptation is performed only on the basis of made decisions ($I(k)$), during the equalization of a priori unknown signal, system completely operates in "blind" mode of equalization. Error signal is multiplied with small value of multiplication constant μ; the value of μ describes dynamics of adaptation and determines residual error after coefficients' convergence ends. Larger values of μ lead to faster convergence of equalizer structure, but also result in higher amount of residual equalization error, or even divergence. Multiplication constant's value that lead system in stable convergence may be evaluated according to [12]:

$$\mu = \frac{1}{(2N+1)E[|u|^2]} \quad (5)$$

where term $E[|u|^2]$ describes average power of signal at input of equalizer. In practice, slightly lower values are used than described by eq. (5). Optimum value of μ for particular application is usually explored through simulations or laboratory experiments – using later approach, we found that $\mu = 2,3 \cdot 10^{-7}$ represents the value that satisfies demands of convergence with acceptable equalization quality. This value is stored within 23-bit register as unsigned all-fractional number. Since significant digits of product $\mu \cdot \varepsilon(k)$ cover wide range of values, but can be restricted on values down to 10^{-5} if only the influence of highest decades in $\varepsilon(k)$ is observed, these values can be formed at 16-bit registers (1 bit for sign, and 15 bits for fractional part of number having precision of 10^{-5}). This product is used for adaptation of coefficients in both FF and DF section.

To complete adaptation signal in FF block it's necessary to multiply generated product with samples of input signal present at filter taps; signals created in this manner can, once again, be restricted on narrower range in order to save logic. If 11-bit registers for results of multiplication at this point are assumed, formed data have precision of 10^{-3}, what is quite appropriate in terms of expected coefficients' values. As it

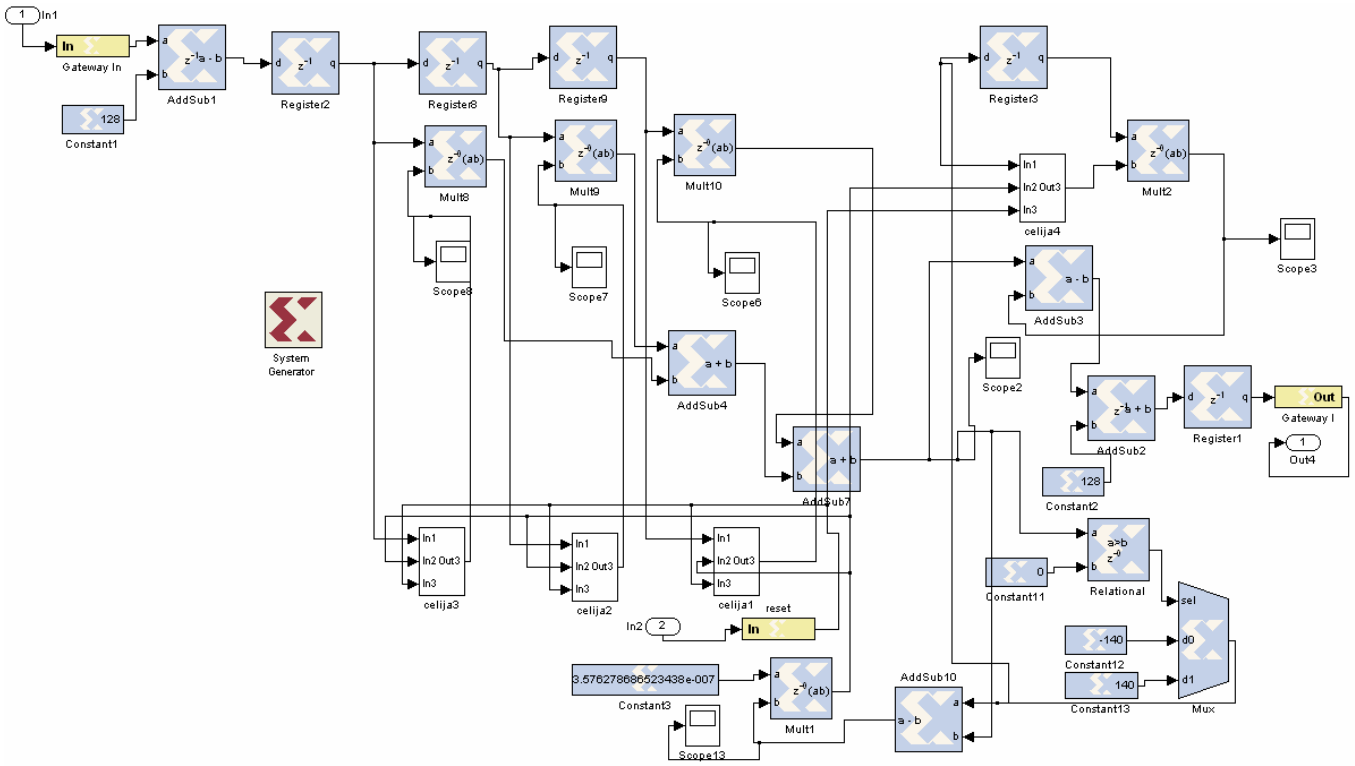

Fig. 2 Digital structure of adaptive equalizer designed in System Generator software.

was previously mentioned, equalizer is intended for operation in "blind" mode – this is why one of FF coefficients is initialized with value "1", while other two FF coefficients are initialized with zeroes. Filter tap that corresponds to first coefficient has the role of "reference" tap, while other two taps are used for equalization of sample present at reference position. Because of this, signed values of later two coefficients can be formed within 12-bit registers with 10 bits for fractional part of numbers, while reference tap coefficient should be stored at 13-bit register (having also 10 bits for fractional part of number), since its value during convergence can easily outrange 12-bit structure.

The situation at DF section is similar. Decisions $I(k)$ are propagating through tap-line of this section, and are being used in every cycle of system clock for adaptation of coefficients B_i, in the manner described by eq. 3. Since the main goal of this research was exploring the structure with minimum complexity that satisfies demands in terms of efficient equalization, we have focused on design with only one tap in DF section. Initial value of only existing coefficient of DF section is "1", and it implicates the width of register where it's stored: generated product that represents adaptation signal is signed 11-bit (10 bits for fractional part) value, while 13 bits (10 for fractional part) are provided for DF coefficient value, just like in the case of "reference" FF tap. It was previously mentioned that value of $y(k)$ can be formed within 9 bits, if output of DF block is kept at enough low level. Savings in logic are not strongest motivation for reduction of value leaving DF section: it is important to prevent DF section in taking the dominant role in process of convergence (which can lead to "oscillations" in $y(k)$, and complete loss of functionality), and the natural approach is to reduce its values at applicable low level. This can be done at the point of multiplication of DF coefficient with decision signal – reducing the value of product on 4 bits (signed number, no fractional part) ensures that it will contribute to value of result of equalization with less than 10% in comparison with signal from FF block. As a consequence of this approach, additional savings in logic are achieved.

As final result, only most significant bit of $I(k)$ can be routed to the output port of adaptive equalizer, since it contains the information about the sign of made decision, and represents binary value of one bit that entered equalizer, after the process of equalization. Also, values of $y(k)$ can be routed to external DA converter in order to be observed with oscilloscope, so the efficiency of reduction of intersymbol interference can be analyzed.

III. IMPLEMENTATION

Digital structure of adaptive equalizer described above has been created with System Generator, application that runs under MATLAB's Simulink [13] and may be used for performances exploration of different digital structures and further execution of VHDL code (corresponding to analyzed structure), intended for implementation on Xilinx's FPGA devices [14]. Design of digital structure of adaptive equalizer is given in Fig. 2. Input port of equalizer is marked with

"Gateway in" block (at the left in Fig. 2), while output port is marked with "Gateway Out" block (at the right in Fig. 2). All particular blocks used in this design correspond with realistic resources present within FPGA chip selected for implementation. Basic building blocks are coloured in light-blue (registers, adders/subtracters, muxes, multipliers), while blocks for adaptation of values of tap coefficients (named "celija1",...,"celija4" in Fig. 2) are coloured in white. Structure of these cells is presented in Fig. 3.

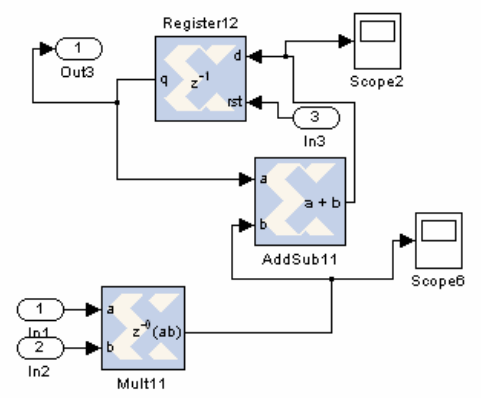

Fig. 3 Cell for adaptation of values of tap coefficients.

After verification of performances (performed in System Generator during simulations with various test-stimulus), executive code is generated and described digital structure is implemented on Spartan 3 FPGA (xc3s200 [14]), within the larger structure that contains two adaptive equalizer blocks, logic for clock distribution, for control of external PLL with VCO circuitry, and blocks for serialization and demultiplexing of signals from two equalizer blocks. This system describes complete logic necessary for independent adaptive equalization of baseband signal in both branches with quadrature modulation scheme. Although the presence of blocks other than equalizers also has influence on amount of occupied resources and maximum speed of operation, this influence is negligible in comparison with equalizer structures. Complete design has been synthesised with XST tool, and implemented on FPGA in ISE 9.1 Webpack environment. Results of implementation are presented in Table I.

TABLE I
RESULTS OF IMPLEMENTATION ON SPARTAN 3 FPGA XC3S200

Resource	Used	Available	Utilization
Slices	957	1.920	49%
4-input LUTs	1.585	3.840	41%
IOBs	50	97	51%
MULT18x18s	10	12	83%
GCLKs	2	8	25%
Total gate acc.	59.315		
Max clock freq.	19.23 MHz		

For achieving maximum speed of operation, embedded multiplier components of FPGA are used (MULT18x18) for implementation of multipliers on critical paths, while other multiplier units can be implemented in form of cores. Clocks for two equalizer blocks are derived from single clock operating at two times symbol rate frequency and routed to equalizers via independent global clock lines (GCLKs), while number of occupied input/output blocks (IOBs) is smaller than reported in case when there is no interest in routing complete bus of equalizer outputs in order to observe full scale values.

As it can be noticed at this point, presented structure efficiently fits in available resources of standard FPGA; achieved maximum speed of operation, having value of 19.23MHz for system clock frequency, is sufficient for operation over I and Q branch of QPSK signal within medium-capacity microwave radio at bitrates up to, approximately, 38.5 Mbit/s. In practice, this means that signals having bitrates up to E3+E1 multiplex can be equalized with this structure, implemented on selected chip. Usage of more advanced FPGAs would result in even higher values of maximum operating speed – for example, approximately two times faster if implemented on Virtex 5 FPGA.

Block scheme of complete adaptive equalizer unit, containing programmed FPGA device and all additional external components is given in Fig. 4. Input signals for complete unit are I and Q branch of E3+E1 multiplex QPSK signal in baseband. After appropriate analogue buffering and filtering, these signals are amplitude-scaled within automatic gain control (AGC) blocks, and then converted in digital signals (A/D converter block) which are routed to FPGA. After being processed by digital adaptive equalizers, signal's samples are arranged in separate E1 and E3 arrays and transferred to corresponding line interface (LI) units.

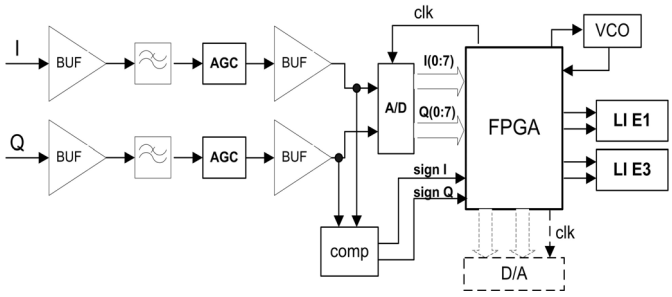

Fig. 4 Block scheme of complete adaptive equalizer unit.

IV. RESULTS

Implemented solution has been tested during laboratory measurements of M-curve signature, performed with E3+E1 capacity digital microwave radio. System performance under conditions of frequency selective fading was explored in two cases: without any protection involved, and with adaptive equalizer described in this paper, implemented on Spartan 3 FPGA. While the presence of ISI was explored through analysis of signal eye-pattern with digital oscilloscope, precise information about signal quality in terms of bit error rate (BER) was observed with BER tester units. Measurement method is shown in Fig. 5.

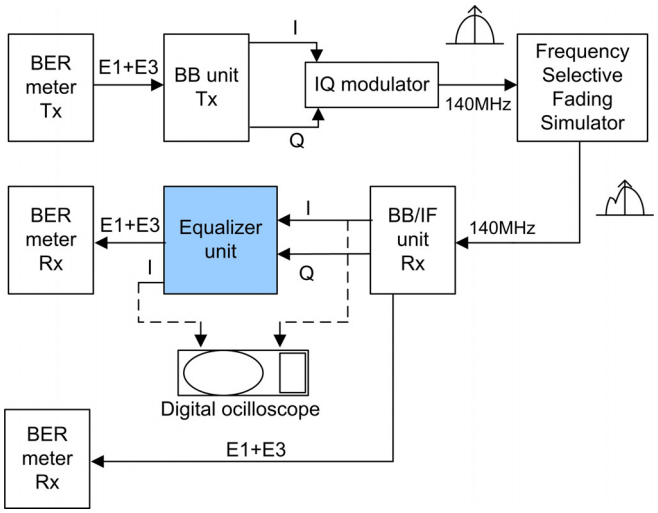

Fig. 5 M-curve signature measurement method.

During these tests functionality of adaptive equalizer structure presented in this paper has been finally confirmed: first, eye-patterns of signal degraded by notch filters around receiver's intermediate frequency (140 MHz), of both minimum phase and nonminimum phase type, for various notch frequencies and depths, has been observed with digital oscilloscope at points prior and after equalization. Since equalizer demonstrated ability to fight ISI during this initial test, in-depth analysis was performed by automated M-curve signature measurements [15]. Eye-pattern of signal degraded by minimum phase notch at frequency 133MHz and having depth of 26dB, before and after equalization, is presented in Fig. 6.

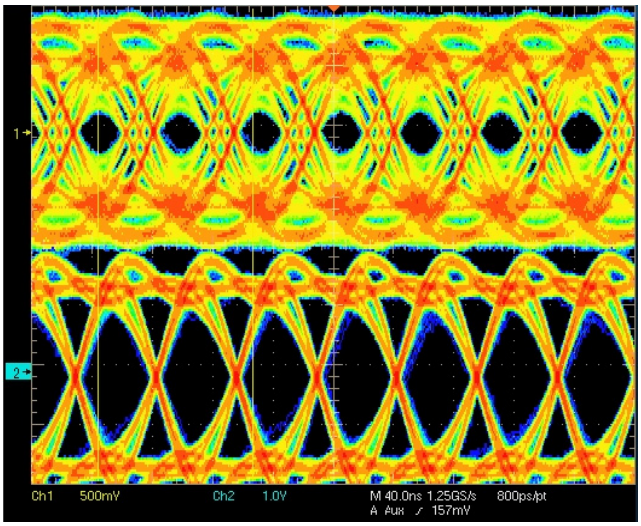

Fig. 6. Eye-pattern of signal before (up – $BER \sim 10^{-3}$) and after equalization (down – errorless transmission); notch freq. 133MHz, notch depth 26dB, minimum phase fading.

M-curve signature measurements, for both minimum and nonminimum phase fades, showed that presence of adaptive equalizer described in this paper increases average value of system signature depth for more than 5dB and reduces signature width for more than 3 MHz. Digital microwave radio with this equalizer included has signature depth of 27.3dB and width of 22 MHz, which is completely satisfying in terms of limits defined by [3] – at least 14dB of signature depth at 30 MHz bandwidth around channel centre frequency for Class 1 systems with E3 bitrate (28MHz channel spacing). This value can be used for the purpose of calculation of dispersive fade margin, according to [4], which yields to DFM=54.3dB for system with adaptive equalizer included. In addition to strong satisfaction of recommended limits, one can notice that achieved results are quite comparable with reported performance in modern digital microwave devices ([6]-[9]). System M-curve signatures in nonminimum phase mode, for cases with and without adaptive equalizer unit present, are given in Fig. 7.

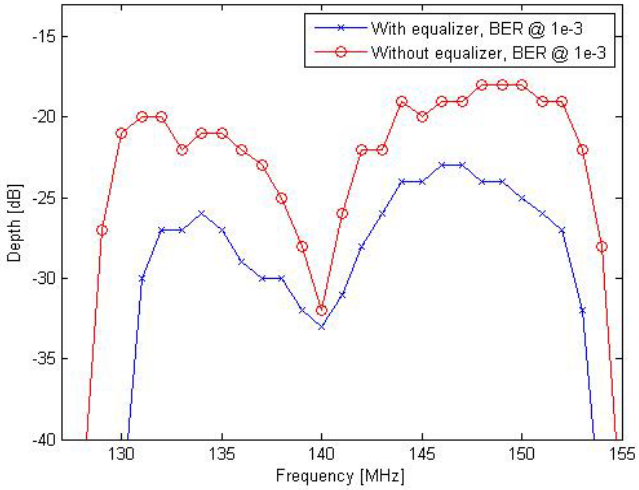

Fig. 7. System M-curve signature, nonminimum phase fading.

Adaptive filters for equalization based on LMS algorithm are favoured by vendors of RR equipment because of their simplicity: the most powerful equalizers, like the one used in PVG modems ([7]) has structure similar to one described in this paper (FF+DF LMS filter), but with significantly more taps – 24 of them. Zero-forcing algorithm [16] is characterised with complexity similar to LMS, but is rarely used in RR devices, since it amplifies the nose together with useful signal in case of deep fading. More effective equalizers, like those with lattice structures, non-linear MAP equalizers, or fractionally-spaced linear filters [17] are also avoided by vendors, because of higher complexity and resource-consuming implementation in digital logic. Structure of digital adaptive equalizer described in this paper is extremely simple, level of demands in digital resources for practical implementation is low, while achieved performance is very satisfying.

CONCLUSION

Solution for realization of "blind" adaptive equalizer with decision-feedback described in this paper is characterized by low complexity, suitable for implementation on standard FPGA hardware. This makes system design, realization and maintenance seriously relaxed, while achieved quality in terms of intersymbol interference reduction showed to be more than applicable for satisfaction of standards. Presented

solution can be used for significant improvement of performance in medium-capacity digital radio systems, but also can be used as a basis for realization of equalizer structures for systems with different particular demands.

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