Performance of OFDM Systems for Broadband Power Line Communications Under Low Signal Strength

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Abstract – **This paper evaluates the performance of OFDM systems for in – home broadband powerline communications when adopting a low signal emission profile. The systems are implemented digitally on Field Programmable Gate Array (FPGA) chips and tested over a real powerline network. Detailed description of the experimental setup and the architecture of the employed systems is also provided.**

Keywords – **Field Programmable Gate Arrays (FPGAs), frequency division multiplexing, power line communications, coupling circuits.**

I. INTRODUCTION

In recent years, the use of indoor power lines for transmitting data and voice has gained rapid interest. The main advantage of power line communications (PLC) is that they exploit the existing wiring of a building. On the other hand, power lines constitute a challenging communication medium in terms of noise, attenuation and multipath propagation. The noise traversing power lines can be characterized as a combination of coloured background noise, narrowband noise and impulsive noise [1]. Powerline noise faces considerably high power strength especially at frequencies below 1MHz. Attenuation is caused by power cable losses that increase with frequency and length [2]. Multipath propagation arises from branching of power lines and unmatched line ends.

Considering power line noise and attenuation, the frequency zone between 1 – 30 MHz is believed to be ideal for the operation of PLC systems [2, 3]. However, this frequency range is used by amateur radio operators, international shortwave broadcasters, and a variety of communication systems (military, aeronautical, etc.), thus a potential for harmful interference with other users exists [4]. Moreover, injecting high frequency signals into the power lines can affect the operation status of apparatus plugged to the network. The maximum levels of conducted emissions over power lines are described in standard EN 55 022 [5]. According to this standard, plc signals should not exceed 1V in peak amplitude. It is doubtful, though, whether reliable power line communications can be set on such signal levels. Homeplug Powerline Alliance suggests higher power spectral density with a maximum value of –50dBm/Hz [6].

For a severe communication environment such as the plc channel, Orthogonal Frequency Division Multiplexing (OFDM) is considered the most favourable modulation scheme [7]. In contrast to the single carrier modulation case, OFDM segments the available bandwidth into a large number of closely – spaced orthogonal subcarriers, each occupying a much narrower bandwidth. In this way, OFDM can combat frequency selective attenuation and multipath propagation effect.

This paper presents the performance of OFDM systems employing low signal power for in – home powerline communications. The systems are evaluated over a real residential powerline network. Every OFDM system consists of a pair of a transmitter and a receiver circuit, which are implemented digitally on two different FPGA chips. The tested OFDM systems differ on the adopted modulation technique and the number of subcarriers used. The choice to develop the communication systems on FPGA chips provides a low – cost, easy to implement, digital solution, and the fact that FPGAs are reprogrammable devices makes possible the reuse of the same FPGA chips for the different OFDM systems. All OFDM systems occupy the frequency zone 1 – 30 MHz. The construction of a suitable coupling circuit to inject (extract) the transmitted (received) OFDM signal into (from) the power lines is also described.

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II. SYSTEM DESIGN

A. Hardware Description

The transmitter and the receiver circuits will each be constructed on two identical XtremeDSP Development Kits of the Nallatech Corporation [8]. This development platform consists of a 105 MHz oscillator that generates the master clock signal of the kit, and two basic FPGAs, a Virtex IV FPGA and a Virtex II device. The Virtex II FPGA can accept an appropriate circuit that uses the kit's master clock to generate clock signals for the different parts of the kit (Virtex IV FPGA, ADCs, DACs, etc.) The Virtex IV FPGA implements the circuit specified by the designer. The transmitter and receiver development kits differ only on the design that the Virtex IV FPGA implements. The designer describes the desired operation of the Virtex IV circuit in a hardware description language (VHDL) and an appropriate software suite is responsible for the transformation of the VHDL commands into the circuit that will configure the Virtex IV FPGA. Two input channels for analog signal reception and two output channels for analog signal emission constitute the interface of the development kit – and consequently of the Virtex IV FPGA – with the communication medium. All input and output channels are terminated with a 50Ω load at MCX type connectors. At each input channel an analog – to – digital converter (ADC) transforms the analog input to 14-bit wide digital signal in two's complement form. The ADC can accept a maximum

input of 4V peak – to – peak and a maximum sample rate of 105 MSPs. At each output channel a digital – to – analog converter (DAC) converts digital, 14 – bit wide, signal in offset binary form to analog output. The DAC has a maximum update rate of 160 MSPs and a maximum output of 4V peak – to – peak.

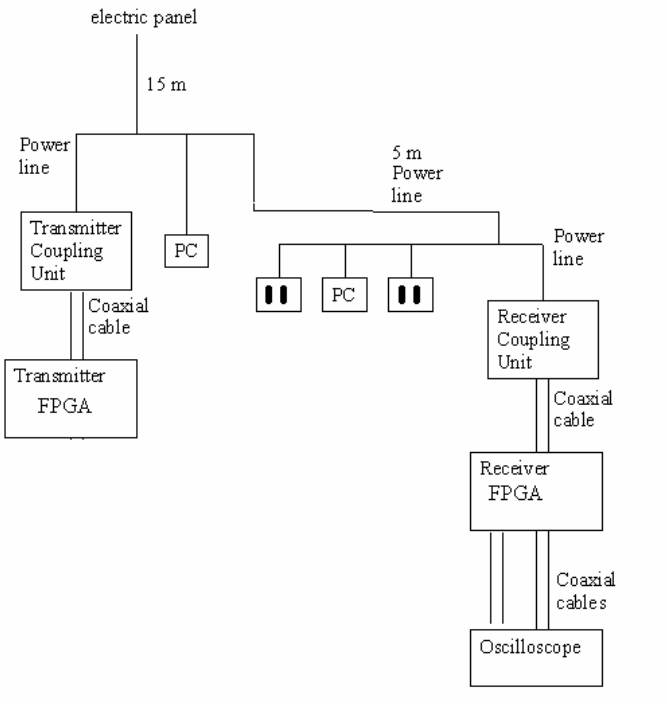

Fig. 1. Setup to evaluate the OFDM systems and powerline network topology.

In order to couple the OFDM signal from the output channels of the transmitter development kit to the power network or decouple the radio signal from the power lines to the input channels of the receiver development kit, a suitable coupling device is constructed. A wideband 1:1 transformer is used to isolate the power line and the communication circuits. The primary winding of the transformer is connected to the power line whereas the secondary winding to the input or output channels of the development kits. The transformer can pass signals from the primary to the secondary winding and vice versa with less than 1 dB distortion in the region 7 kHz to 80 MHz. A 0.5A fuse for safety reasons, a 50Ω resistor for impedance matching purposes, and a 10nF capacitor, eliminating 50 Hz power voltage and noise below 1 MHz, are connected between the power line and the transformer's primary.

Fig.1 shows the experimental setup employed in order to test the performance of the OFDM systems over a real powerline network. At the first output channel of the transmitter development kit the modulated OFDM signal is produced out of a user – defined data sequence. The OFDM signal is passed to the coupling unit through a coaxial cable. The transmitter coupling unit injects the OFDM signal into an F – type socket of a home powerline network. Through another socket of the home network, the receiver coupling unit extracts the OFDM signal and transfers it to the first input channel of the receiver development kit. The receiver development kit processes the received OFDM signal and exports the retrieved data sequence at the first output channel of the kit. The receiver Virtex IV FPGA is aware of the data sequence that modulated the transmitter's OFDM signal, compares the initial with the retrieved sequence and outputs the bit error rate (BER) performance at the second output channel of the receiver's kit. A digital oscilloscope depicts both output channels of the receiver's development kit.

The transmitter and the receiver lie on a distance of 5m along a power line. Several apparatus are also connected to the small home network topology as shown in Fig. 1.

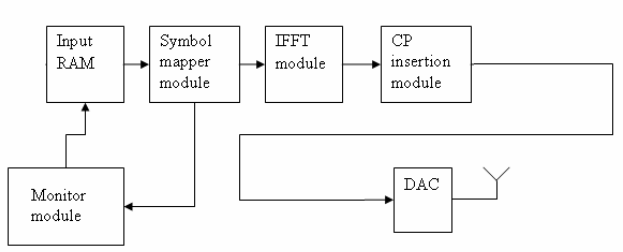

Fig. 2. Block diagram of the architecture of the transmitter circuits.

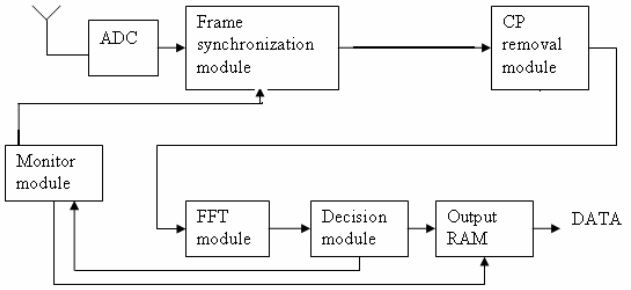

Fig. 3. Block diagram of the architecture of the receiver circuits.

B. Functional Description

The block diagram of the transmitter is depicted in Fig. 2. The transmission of the OFDM signal is not a continuous process, as several OFDM symbols are grouped and sent together in an OFDM frame. The transmitter emits OFDM frames of constant length at normal time intervals. In each frame of M OFDM symbols, the first two symbols are intended for frame synchronization and channel estimation purposes at the receiver, while the rest are payload symbols. The information bit stream is stored at the input RAM. The information stream contains binary data (bit 1 or bit 0). The monitor module adjusts the input data rate by controlling when data samples will be read from the input RAM and sent to the symbol mapper module. The monitor module also supervises the operation of the transmitter circuit by

suspending the generation of the OFDM signal or resuming when desired. The main responsibility of the symbol mapper module is to produce the symbol vector, a sequence that specifies the bits that will be loaded at every subcarrier, according to a mapping method of our choice. The tested OFDM systems use binary phase shift keying (BPSK) or differential phase shift keying (DPSK). The symbol mapper also regulates the number of subcarriers in every OFDM symbol and the number of symbols in every OFDM frame. The symbol mapper module sets the first symbol of every frame as pilot for frame synchronization at the receiver, the second symbol as pilot for channel estimation (for the BPSK case only), and the rest symbols as payload. Finally, the symbol mapper controls the spectrum of the transmitted OFDM signal by zeroing certain carriers. The IFFT module calculates the inverse discrete Fourier transform (IDFT) of every symbol vector, thus producing a sampled version of the transmitted OFDM signal. The cyclic prefix (CP) insertion module adds a cyclic prefix to every produced symbol of the OFDM signal in order to combat the multipath propagation effect. The CP insertion module also specifies the duration of every sample, according to the bandwidth that we wish the transmitted signal to occupy, and forces every OFDM symbol to the DAC, where the analog OFDM signal is generated and emitted through the communication channel.

The architecture of the receiver circuit is given in Fig. 3. The analog transmitted OFDM signal is received through the first analog channel of the kit. The ADC converts the analog signal to a 14 – bit wide digital signal in two's complement. The frame synchronization module seeks among the input samples for the beginning of a new frame. If a new frame has been recognized, the fist symbol is removed and the remaining M-1 symbols of the frame are transferred to the cyclic prefix (CP) removal module. The CP removal module extracts the cyclic prefix from every OFDM symbol and passes every symbol to the FFT module. The cyclic prefix is appropriately removed so that inter-symbol interference due to any FFT window misalignment is unlikely to occur. The FFT module retrieves the transmitted symbol vector by applying the forward discrete Fourier transform (DFT) to the received OFDM symbols. The decision module produces an approximation of the transmitter's input data stream out of every symbol vector, following an inverse procedure to the symbol mapping process of the transmitter. For the BPSK case only, the module exploits channel status information, found in the channel estimation symbol, to reach a decision. The retrieved bit sequence is written to the output RAM. The monitor module controls reading from the output RAM to the DAC so that the output bit rate matches the input bit rate of the transmitter. The monitor module can also suspend or resume the operation of the receiver circuit.

The first OFDM system employs a simplified scheme where the available bandwidth is divided to 16 subcarriers. The OFDM signal occupies the region 4 – 22 MHz. The subcarriers are loaded following binary phase shift keying (BPSK). Every sample has 38ns duration. A 4 – samples (152ns) long guard interval is adopted against multipath propagation effect. A maximum delay spread longer than 152 ns is not expected considering the topology of the tested powerline network [9]. Every frame consists of 4 OFDM symbols of 20 samples each. The first two symbols are pilot, and the rest are payload symbols. The synchronization pilot waveform is a sine of frequency 13.16 MHz. The duration of every frame is 3040ns and the frame inter – arrival time is 3952ns. The system's useful data rate is approximately 3 Mbps.

The second system adopts a scheme based on HomePlug BPL proposed by HomePlug Alliance for powerline communications [3]. BPSK modulation is still employed, but now the available bandwidth is divided to 1024 carriers, and the actual signal's bandwidth lies in the region 1.8 MHz – 24.5 MHz. Every sample lasts for 38ns. Following the suggestions of HomePlug BPL for the guard interval length (5.56μs, 7.56μs, 47.19μs) [10], an interval of 133 samples (5.05μs) is selected. Every frame consists of 4 OFDM symbols of 1157 samples each. The first two symbols are pilot and the synchronization symbol is a sine of frequency 13.16 MHz. Every frame lasts for 175.86μs and a new frame is emitted every 176.78μs. The system's data rate now increases to 5 Mbps.

The third system adopts the specifications described in the second architecture, except for using DPSK modulation instead of BPSK. DPSK modulation does not require a training symbol for channel estimation, so only the synchronization pilot symbol is necessary. Thus, in a frame of 4 OFDM symbols, the three symbols can carry information data. The system's useful data rate now reaches 7.5 Mbps.

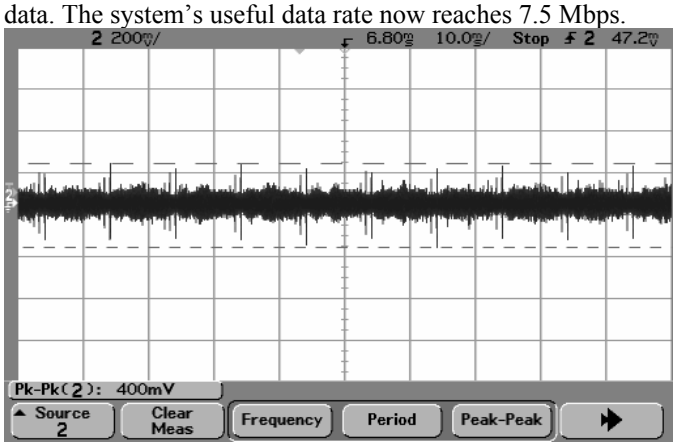

Fig. 4. Screenshot of powerline noise as taken by an oscilloscope.

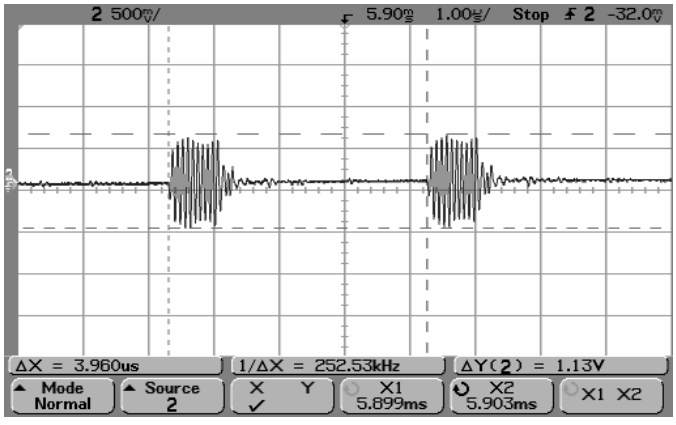

Fig. 5. Signal at the input of the receiver for the 16 – carriers – BPSK system. SNR is measured at 9dB.

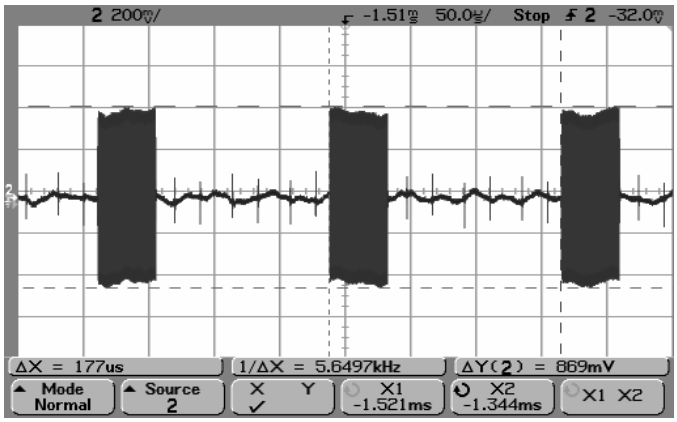

Fig. 6. Signal at the input of the receiver for the 1024 – carriers – DPSK system. SNR is measured at 6.5dB.

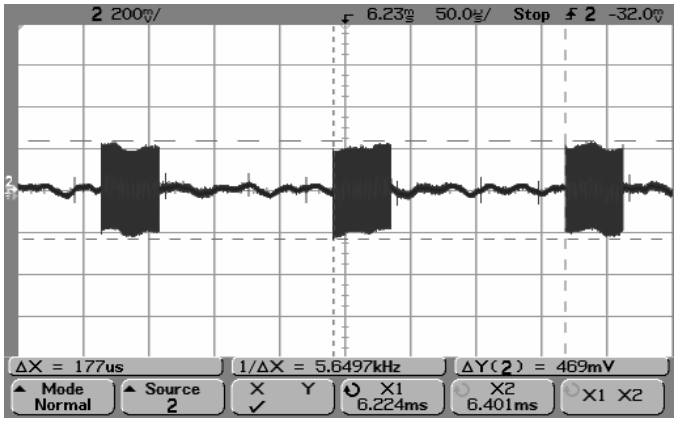

Fig. 7. Signal at the input of the receiver for the 1024 – carriers – BPSK system. SNR is measured at 1.4dB.

III. RESULTS

Fig. 4 presents a screenshot of the noise encountered in the examined residential powerline network, taken by a digital oscilloscope. The colored background noise component and the impulsive noise component of powerline noise can easily be distinguished in Fig. 4. The peak – to – peak amplitude of colored background noise varies between 150mV and 200mV. The average value of background noise is estimated around 180mV peak – to – peak. The impulsive noise component, however, faces higher voltage values. Moreover, the peak – to – peak amplitude of the impulses varies in a much wider range, from 350mV up to 600mV. Occasionally, impulses as high as 1V – 1.5V peak – to – peak can arrive. The average value of impulsive noise is calculated at approximately 400mV peak – to – peak. In the following, the average value of impulsive noise will be considered as the average value of powerline noise. Thus, in our BER analysis, the peak – to – peak voltage of 400mV will be regarded as the noise level.

Figs. 5 – 7 show the received OFDM signal at the input of the receiver for different OFDM architectures and different signal emission levels. The signal at the input of the receiver is measured at 1.13 V peak – to – peak, 850 mV peak – to – peak, and 470 mV peak – to – peak for each signal emission level. Thus, measurements of the performance of the OFDM systems are taken for signal – to – noise ratios (SNRs) of 9dB, 6.5dB and 1.4dB respectively. Figs. 8 – 10 present the retrieved data sequence at the output of the receiver for an input data sequence of alternating bits 1 and 0. Figs. 8 – 10 verify that the data rate for the 16 – carriers – BPSK system is approximately 3Mbps, for the 1024 – carriers – BPSK 5Mbps and 7.5Mbps for the 1024 – carriers – DPSK system.

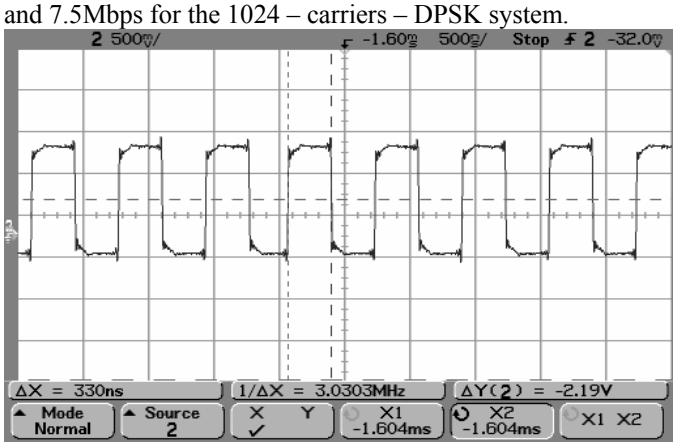

Fig. 8. The output of the first channel of the 16 – carriers – BPSK receiver kit as depicted by the oscilloscope.

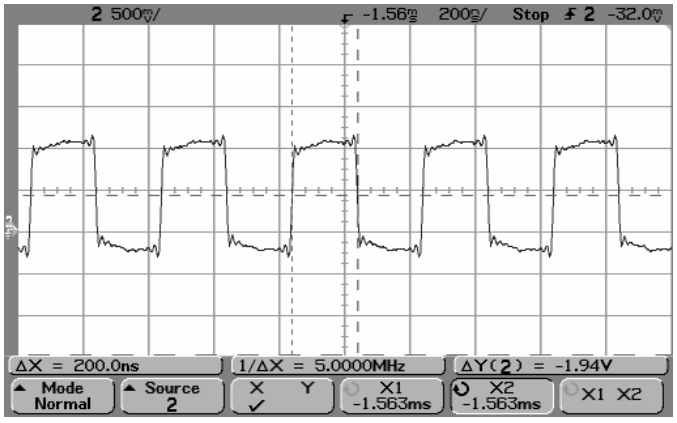

Fig. 9. Retrieved data sequence at the output of the receiver development kit for the 1024 – carriers – BPSK system.

Fig. 10. Output of the first channel of the receiver kit for the 1024 – carriers – DPSK system as shown by the oscilloscope.

Fig. 11 presents the bit error rate (BER) performance of the OFDM systems under different signal – to – noise ratios. The first OFDM system employs 16 carriers and BPSK modulation, the second 1024 carriers and BPSK modulation

and the third 1024 carriers and DPSK modulation. The BER for the 9dB case varies between 0.4% and 5.8%. For the cases of 6.5dB and 2.6dB, the BER range is 0.6% - 6.8%, and 3.9% - 11.9% respectively. It is obvious that the bit error rate performance of all OFDM architectures improves as the signal – to – noise ratio increases.

Fig. 11 also reveals that the 16 carriers – architecture outperforms the 1024 – carriers – BPSK and the 1024 – carriers – DPSK OFDM systems. Since multicarrier systems adapt better to channel variations as the number of subcarriers increases, it would be expected that the 1024 – carriers architectures would perform better than the 16 – carriers system. However, under low signal emission conditions, the influence of powerline impulsive noise becomes a more crucial factor for system performance than frequency dependent attenuation and multipath propagation effect. It has been proved [11] that when the strength of impulsive noise is comparably high, namely roughly SNR<10dB, the performance of OFDM systems deteriorates as the number of carriers increases. In multicarrier systems, the energy of impulsive noise is spread over all the subcarriers. As the number of subcarriers increases, the impulsive noise energy at each subcarrier decreases to lead a better BER. On the contrary, a higher number of subcarriers means larger OFDM symbol duration. As the symbol duration increases, the average number of impulses per OFDM symbol increases as well, leading to a worse BER. When SNR is high, the DFT can effectively suppress the impulsive noise energy to reduce the number of errors. So, as a result, the BER can be improved as the number of subcarriers increases. In our case, however, where SNR is low, the OFDM systems cannot suppress the impulsive noise energy below a suitably low level, so the DFT operation results in errors over all the subcarriers. Thus, if the number of subcarriers decreases, the effect of impulsive noise can be limited to fewer carriers within a few symbols leading to a better BER performance.

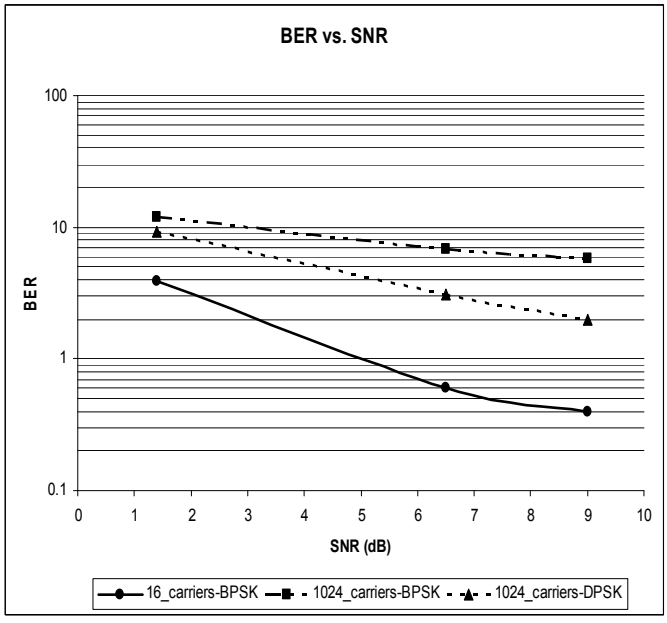

Fig. 11. Analytical BER performance of the three OFDM systems under varying SNR.

Another cause for BER degradation in the tested OFDM systems is frame synchronization offset errors, namely errors in specifying with accuracy the boundaries of DFT windows at the receiver. Timing offset errors are more often as symbol duration – and consequently frame duration – gets larger. In the evaluated OFDM systems, the cyclic prefix of every symbol is removed in such a way that FFT window misalignment into the next OFDM symbol is unlikely to occur. FFT window misalignment is likely to take place only towards the cyclic prefix of the same symbol. If the FFT window captures d samples from its own cyclic prefix, data carried by the k-th subcarrier (in total of N subcarriers per symbol) will experience a face shift of $-\frac{2\pi}{N}\cdot k\cdot d$, following the circular shift property of the DFT. However, if differential PSK modulation is employed instead of BPSK, adjacent carriers will experience a constant phase shift of $-\frac{2\pi}{N}\cdot d$, irrespective of subcarrier position within the OFDM symbol. Thus DPSK systems are more robust against frame synchronization errors compared to BPSK systems. This result is verified by Fig. 11, where the 1024 – carriers – DPSK system outperforms the 1024 – carriers – BPSK system, for all SNR values.

IV. Conclusion

We have presented the results of an implementation-based study carried out to investigate the BER performance of OFDM systems over the residential power supply network under low signal emission conditions. It has been shown that OFDM systems can perform under emission levels specified by existing standards. However, complying with existing standards results in increased BER. Under these conditions, it has been proved that OFDM systems with fewer carriers perform better because they are less affected by impulsive noise. DFT window timing error is another crucial issue regarding the performance of real powerline OFDM – based systems. It has been shown that DPSK modulation can reduce the influence of timing synchronization error to BER performance, when compared to BPSK modulation.

Acknowledgement

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References

[1] M. Zimmermann, K. Dostert, “Analysis and Modeling of Impulsive Noise in Broad-Band Powerline Communications”, *IEEE Trans., Electromagn. Compat.,* vol. 44, no. 1, pp. 249-258, 2002.

[2] M. Gotz, M. Rapp, and K. Dostert, “Power Line Channel Characteristics and Their Effect on Communication System Design”, *IEEE Commun. Magazine,* vol. 42, no. 4, pp. 78-86, 2004.

[3] HomePlug Powerline Alliance: HomePlug AV White Paper. www.homeplug.org/products/whitepapers/HPAV-White-Paper_050818.pdf.

[4] M. Zhang, W. Lauber, "Evaluation of the Interference Potential of In – Home Power Line Communication Systems ", *IEEE*, *International Symposium on Power Line Communications and Its Applications*, pp.263-268, Jeju Island, Korea, 2008.

[5] CENELEC EN 55022: Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement. www.cenelec.eu.

[6] M. Ouzzif, J. Le Masson, "Channel Capacity Statistical Analysis for Indoor Power Line Transmissions", *IEEE*, *International Symposium on Signals, Systems, and Electronics,* pp.575-578, 2007.

[7] N. Pavlidou, A. Han Vinck, J. Yazdani, and B. Honary, "Power Line Communications: State of the Art and Future Trends", *IEEE Commun. Magazine,* vol. 41, no. 4, pp. 34-40, 2003.

[8] Nallatech Ltd.: XtremeDSP Development Kit – IV User Guide. www.nallatech.com.

[9] M. Zimmermann, K. Dostert, "A Multi-Path Signal Propagation Model for the Power Line Channel in the High Frequency Range", *ISPLC'99*, *Conference Proceedings*, pp.45-51, Lancaster, UK, 1999.

[10] H. Latchman, K. Afkhamie, S. Katar, R Newman, B. Mashburn, and L. Yonge, "High Speed Multimedia Home Networking over Powerline", *National Cable and Telecommunications Association (NCTA)*, *National Show*, April 2005.

[11] S. Hara, R. Prasad, *Multicarrier Techniques for 4G Mobile Communications,* Boston, Artech House, 2003.