Electromagnetic Interference and Start-up Dynamics in High Frequency Crystal Oscillator Circuits

Ulrich L. Rohde, Ajay K. Poddar, Rucha Lakhe

Abstract – **An oscillator circuit is commonly a significant source of radiated emission in electronic systems. Crystal oscillators, which have been widely used as a reference frequency standards, are susceptive to electromagnetic interference (EMI), drive-level, and start-up dynamics. The effect of radiated EMI can be both deterministic and random in nature, which shows up as jitter in the time domain and translates into the phase noise in the frequency domain. If the impact of EMI is too large, the performance of the entire system would be affected in terms of accuracy, stability, start-up, and phase noise. Experimental results and CAD simulated data provide insights into EMI and start-up dynamics and validated with the design example of 100 MHz crystal oscillator.**

Keywords – ***CAD, Crystal Oscillator, Jitter, EMI, Phase Noise***

I. INTRODUCTION

Electronic devices/modules typically generate undesirable electromagnetic energy. This electromagnetic (EM) energy often generates an unwanted EM field or a transient within the RF band (10 kHz - 10 GHz) of the EM spectrum and are commonly referred to as EMI's (Electromagnetic interference). Such electromagnetic interference (EMI) is being known to interfere with the designated operation of the electronic circuitry of other proximate electronic devices [1]. Radio frequency interference (RFI) is often used interchangeably with EMI, although it is restricted to the radio frequency (RF) portion (10 kHz - 10 GHz) of the EM spectrum. Reference frequency standard such as crystal oscillator circuit, which oscillates at radio frequency (RF) is sensitive to conducted (as referenced in Fig. 5) and radiated (as referenced in Fig. 6) EMI from external and internal RF and EM fields [1]-[24].

Furthermore, current trend of developing compact and integrated high frequency signal sources invite undesired EM coupling that plagues the neighboring electronic components/circuits, produces deleterious EMI due to the increased number of electronic components located within the electronic devices. EMI protection is critical in compact densely packaged, crystal oscillator circuits operating at VHF/UHF for the applications in RF & MW communication systems. As consumer electronic products become price sensitive, smaller, faster, and more complex, the system designer must consider efficient and cost-effective ways to minimize the resultant rise in EMI due to conduction and external radiation. Furthermore, EMI related problems are typically not addressed until the final stages of the design/development cycle, and are consequently time consuming and expensive to locate and minimize. Therefore, due care must be taken for not only meeting the product specifications but also creating the most reliable end product by limiting the negative influence of EMI, both emitted and received [1]-[11].

A number of international government agencies impose guidelines on the allowable EMI that electronic modules can emit. In the United States of America (USA), the Federal Communications Commission (FCC) has divided EMI for computing electronic devices into two categories: (1) Radiated and (2) Conducted Emission. Table 1 lists the maximum permissible Radiated Emission (RE) interference from the electronic devices, measured in terms of Electric Field Strength [24]. The maximum permissible limit of Conducted Emission (CE) interference is typically 260 μV over the frequency range of 450 kHz to 30 MHz, and related with the noise interference fed back to the power supply lines [20]-[24].

To meet the FCC regulations, most electronic devices/equipments/systems including crystal oscillator circuits' currently employ a combination of two approaches (source suppression and containment) depending upon the cost factor and tolerable limit of the EMI [19]-[21]. The source suppression techniques enable the design methodology in such a way that only essential signals are to be present in signal interconnections, and unwanted EM energy restricted either by not being generated or attenuated before it leaves the device/component/equipment/sub-system.

TABLE 1
RADIATION LIMITS FOR CLASS B
COMPUTING DEVICES (FCC RULES)

Freq. (MHz)	Distance (M)	Field Strength (μV/m)
30-88 MHz	3 Meter	100 μV/Meter
88-216 MHz	3 Meter	150 μV/Meter
216-1000 MHz	3 Meter	200 μV/Meter

Whereas, containment technique attempts to place a barrier around the assembled electronic components, subsystems, interconnections, etc., thereby restricting the unwanted EM energy within the boundaries of the product, where it can be

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dissipated without plaguing neighboring electronic devices/sub-systems/equipments.

A. Noise Interference Sources and Propagation Channel

Identification and localization of noise interference sources in electronic devices/modules/equipments, including crystal oscillators is critical task for designing low EMI electronic products. Figure (1) shows a typical block diagram of the noise interference source model of a video graphics system [24]. As described in Figure (1), the first task is to eliminate (if possible) the particular noisy circuit from the design flow chart, thus avoiding additional filtering, which otherwise would be needed later to minimize the noise interference. But in reality, it is not easy steps to eliminate all the components/modules that are responsible for generating or propagating unwanted noise interference because they may be critical modules for the designated functionality. However, by being aware of their locations in the design flow chart, partial effects can be minimized at the source and in the coupling channel by using optimum filtering and decoupling circuit networks.

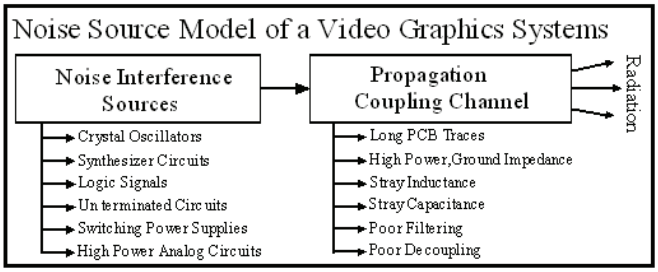

Fig.1: A typical block diagram of noise source and propagation model.

B. Example of Crystal Oscillators & Associated Network

A typical video system usually comprises of a number of crystal oscillator modules varying in frequency from 20 MHz to 200 MHz, including clock and pixel data circuits, which are required to formulate different pixel resolutions on screen for display. These crystal oscillator modules and their associated circuitry tend to be rich in noise and harmonic components at low current drive-level and high operating frequency, and are the prime source of electromagnetic interference (EMI). The general guidelines for designing EMI insensitive signal sources, including crystal oscillators are given below:

- Crystal oscillators should be placed as far as possible from the analog circuitry and video output connectors.
- With reference to low EMI crystal oscillator design, the transition time (rise/fall time) must be symmetric to minimize the unwanted harmonics and modes.
- Mixing of clock buffers and other logic modules in the same IC package should be avoided.
- Several low power data drivers or buffers for the clock and pixel data lines distributed throughout the board should be used in comparison to a single power driver.
- Power supply to crystal oscillator circuit must be isolated by using ferrite beads.

Figure (2) shows the typical schematic of 100 MHz Butler crystal oscillator circuit. A typical Butler oscillator or the bridged-T oscillator topology is a family of low noise crystal oscillators in which emitter current passes through the crystal resonator, resulting near sinusoidal output waveform. This in-built filtering action improves the phase noise outside the effective bandwidth of the crystal's resonant frequency, *f*, by operating loaded quality (Q) factor.

However, as operating frequency increases, the unwanted harmonic components become more predominant, causing increase in the noise interference levels as well as poor phase noise performance. Figure (3) shows the typical CAD simulated plot of the output spectrum of 100 MHz Butler crystal oscillator. As shown in Figure (3), the first harmonic level is typically 12dB below the fundamental frequency of 100 MHz, thus has inferior phase noise performances (Fig.4).

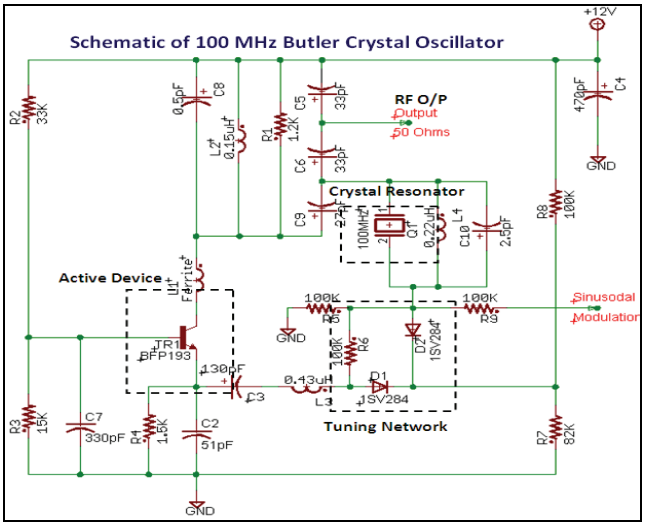

Fig.2 Typical schematic of 100 MHz Butler Crystal oscillator circuit

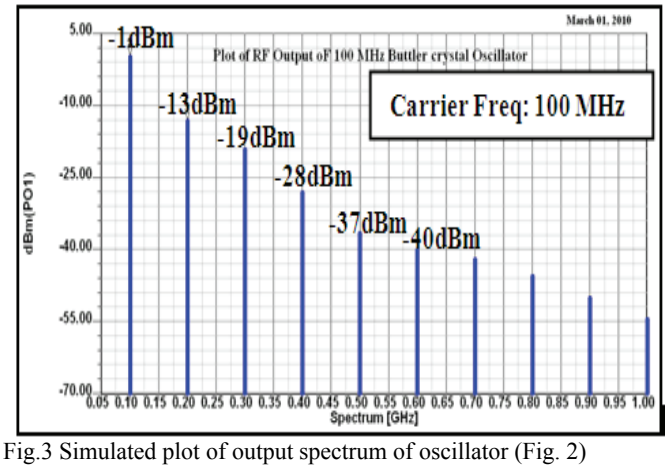

Fig.3 Simulated plot of output spectrum of oscillator (Fig. 2)

For comparative analysis, we are reporting the typical schematic of differential-coupled phase-injection locked 100 MHz crystal oscillator circuit (shown in Fig. 5). The simulated output spectrum and phase noise performance is superior to the Butler topology as shown in Figure (2). Figure (6) shows the simulated plot of the harmonic contents, the first harmonic level is typically 29 dB below the fundamental frequency 100

MHz, thus improved phase noise performance (shown in Fig. 7) as compared to the typical phase noise plot of Butler oscillator (Fig. 4).

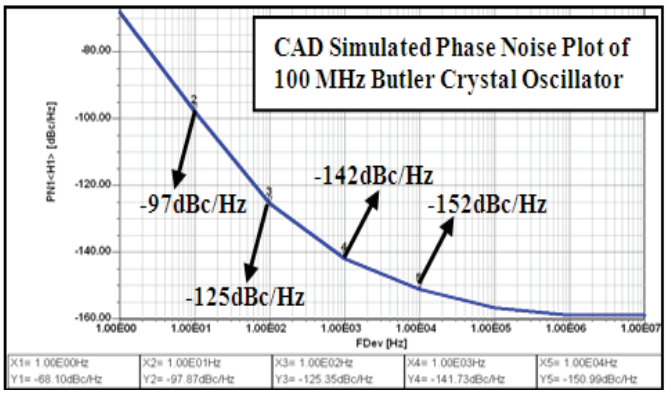

Fig.4: The simulated phase noise plot of Butler oscillator (Fig. 2)

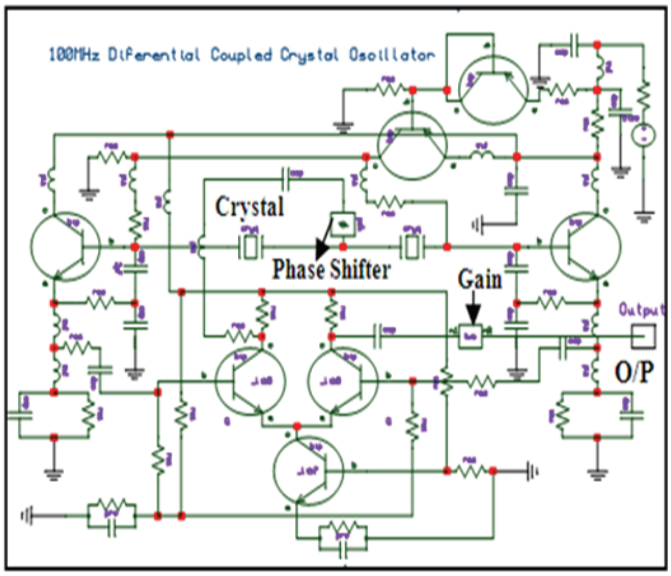

Fig.5 A typical schematic of 100MHz differential coupled oscillator

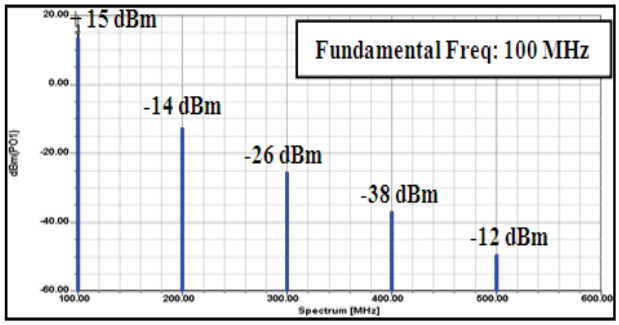

Fig.6 A typical simulated plot of output spectrum of oscillator (shown in Fig. 5)

Furthermore, Figure (7) shows the simulated phase noise plot of the differential coupled oscillator with and without gain block for insights about the rise in noise floor due the inclusion of amplifier module at the output for improved isolations. In addition to this, influence of conduction noise due to bias network is studied.

Figure (8) shows the simulated phase noise plot of the 100 MHz differential coupled oscillator using both fixed and self-biasing techniques for the qualitative analysis of the noise contribution due to conductive interference fed back onto the power supply through biasing of the crystal oscillator circuit.

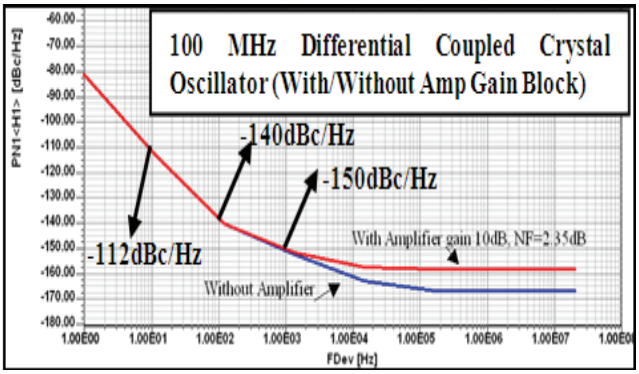

Fig.7 A typical CAD simulated phase noise plot of the 100 MHz crystal oscillator circuit with and without amplifier gain block.

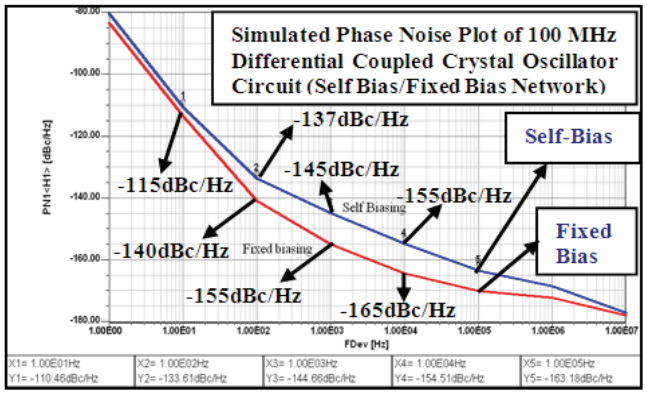

Fig.8 A typical CAD simulated phase noise plot of the 100 MHz crystal oscillator circuit with fixed and self-biasing network.

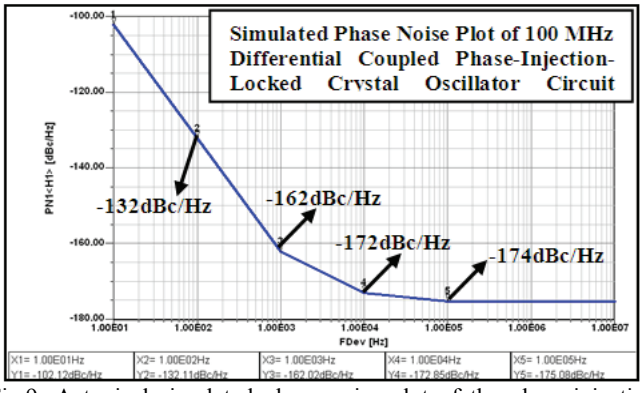

Fig.9: A typical simulated phase noise plot of the phase-injection locked differential coupled oscillator circuit (Low EMI Topology)

Figure (9) shows the phase noise plot of the phase-injection-locked differential coupled crystal oscillator circuit, the simulated phase noise is -162dBz/Hz at 1 kHz offset from the carrier. It can be seen from Figure (9), the simulated phase noise at 1 kHz offset is 10-20 dB superior in performance as compared to conventional Butler topology (Fig. 2).

C. Printed Circuit Board (PCB) and Associated EMI

The printed circuit board (PCB) acts as a propagation channel for unwanted noise sources and couples this unwanted noise interference onto other peripheral circuitry, leading to the radiation of generated EMI into free space. The main causes of EMI due to PCB are following [24]:

- Common impedance coupling via power and ground traces.
- Antenna loops formed by ICs and their bypass capacitors, which include power and ground leads.
- Printed circuit board traces carrying signal currents.
- Crosstalk between adjoining signal traces.

In general, power supply decoupling holds the transient currents up to some extent within the bypass loop. However, significant parts of the high frequency components tend to escape onto the power and ground traces. In order to avoid common impedance noise coupling due to these currents, care must be taken to reduce the impedance of the power and ground traces to minimum value.

The simplified approach to overcome this problem is to avoid use of power and ground planes (2-layer or multi-layer PCB) instead of traces. A typical 4-layer board with power and ground plane "sandwich" inside the board with the signal trace on the top and bottom, results in intrinsic high frequency decoupling. Due to the overlapping, power and ground planes act as an inherent distributed capacitor, thus they result in decoupling.

Keeping into the consideration of interconnects the main advantage of ground plane is the substantial reduction in signal loop area that it supports. In a typical PCB layout, signal current flows out through one trace and returns through a ground trace, resulting high inductance for the traces with follow-on consequences of signals ringing, EMI radiation and crosstalk. The design objective is to reduce the inductance by reducing the loop area through which the signal current flows.

In addition to this, stray inductance and capacitance can cause signals to ring, to overshoot or undershoot the steady state voltage levels, This kind of ringing phenomena is a main source of EMI which can be minimized by keeping wires or traces short and adding series, damping resistance at the source or termination of long signal paths. Furthermore, unterminated circuits with floating signal lines should be avoided otherwise may lead to unwanted oscillations.

D. Impact of EMI on Crystal Oscillator and Shielding

The impact of EMI radiation can be prevented from entering the device and interfering with its operation by incorporating effective shielding, which has capability of absorbing and/or reflecting EMI energy. Furthermore, shielding can be incorporated to confine the EMI energy within a source device and also to insulate the device or other target devices from other potential source devices.

In particular, shielding is designed to prevent both ingress and egress of electromagnetic energy relative to a housing or other enclosure in which the electronic equipment is disposed but needed additional real estate area for metallic enclosure that encompass electronic components. But the effectiveness of the shielding depends upon the permeability and conductivity of the shielding material, and a frequency and wave impedance of the signal.

II. EMI, JITTER AND PHASE NOISE

The high frequency crystal oscillator is more susceptive to time domain jitter and frequency domain phase noise, which directly affects the stability or accuracy of the reference frequency standard in a communication system [26]. There are a number of factors that contribute to jitter that includes broadband noise, spurs, slew rate, bandwidth, and EMI. The broadband noise is random in nature, whereas spurs are deterministic responses caused by various identifiable interference signals such as EMI, crosstalk and power supply coupling as shown in Figure (10).

Electromagnetic Interference (EMI) can be both deterministic and random in nature, which shows up as jitter in the time domain and phase noise in the frequency domain. Figure (11) shows the typical representation of the external noise sources (EMI and other noise sources) impacting oscillator noise dynamics.

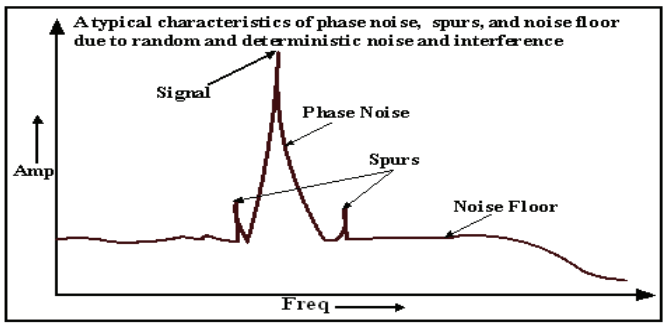

Fig. 10: A typical characteristics of phase noise, spurs and noise floor

III. EMI DESIGN CONSIDERATION IN CRYSTAL OSCILLATORS

The EMI generated by crystal oscillator is the result of high frequency currents in the oscillator circuit. To minimize the EMI, the layout of the crystal oscillator circuit on the printed circuit board (PCB) is designed in such a way that effective loop area (S) where RF current flows to be kept relatively small. In this case, when measuring electric field from a far distance, the loop can be considered as a magnetic dipole and the expression for electric field can be given by $E(r,\theta,\varphi)$ [23]

$$\mathrm{E}(\mathrm{r},\theta,\phi) = \hat{\mathrm{a}}_{\mathrm{r}}\mathrm{E}_{\mathrm{r}} + \hat{\mathrm{a}}_{\theta}\mathrm{E}_{\theta} + \hat{\mathrm{a}}_{\phi}\mathrm{E}_{\phi} \tag{1}$$

$$\left|\mathrm{E}^{\mathrm{far}}\right|_{\max} = (1.317\times10^{-6})\left[\frac{\mathrm{I(f)}\times\mathrm{S}\times\mathrm{f}^2}{\mathrm{R}}\right]\times\left[1+\frac{(\lambda\tau\,\mathrm{R})^2}{2}\right]^{1/2} \tag{2}$$

$$\mathrm{B} = \mu_0\,\mu_{\mathrm{r}}\mathrm{H} \cong \mathrm{I(f)}\times\mu_0\times\mu_{\mathrm{r}}\left[\frac{1}{4\pi r^2}\right](\mathrm{T}), \quad \mu_0 = 4\pi\times10^{-7} \tag{3}$$

$$2\pi\left[\frac{r}{\lambda}\right] << 1 \tag{4}$$

Where $I(f)$ is the current component at frequency f, S is area of the loop, λ is the wavelength at the frequency of interest, μ_r is the relative permeability, H is the magnetic field intensity, and R is the distance from the center of the magnetic dipole on the oscillator printed circuit board (PCB). The expression for magnetic field is given by eqn. (3), where l is the equivalent length of the wire that comprises the loop on the layout of the oscillator PCB. The measured field is considered as a close field when eqn. (4) holds, where r is the distance of the RF probe's head from the line, and λ is the wavelength.

From eqn. (1) - eqn. (4), EMI is in large part a function of current loop area, which can translates into the induced noise voltage as

$$v_n(t) = -\frac{\partial \psi}{\partial t} = -\frac{\partial(\int_s(\overline{B}.\overline{S})}{\partial t} = -\frac{\partial(\int_s(\overline{\mu H}.\overline{S})}{\partial t} \quad (5)$$

Where ψ is the magnetic flux, t is the time, $v_n(t)$ is the induced voltage, B is magnetic flux density, S is the coupling area, H is the magnetic field intensity, and μ is the permeability. The relationship between induced noise voltage and jitter can be expressed by

$$\Delta t_{jitter} = \frac{v_n(t)}{m_s} = \left[\frac{1}{m_s}\right] \times \left[-\frac{\partial}{\partial t}\int_s(\overline{\mu H}.\overline{dS})\right] \quad (6)$$

$$\Delta t_{jitter} = f(v_n) \quad (7)$$

Where m_s is the slew rate and $v_n(t)$ is the EMI induced voltage at the input of a circuit. From eqn. (7), the probability distribution $f(v_n)$ can be given by

$$f(v_n) = \frac{1}{\sqrt{2\pi v_{n(RMS)}^2}} e^{-\left(\frac{v_n^2}{2v_{n(RMS)}^2}\right)} \quad (8)$$

The probability density as a function of the timing jitter Δt is evaluated by setting $v_n(t) = A \sin(2\pi f \Delta t)$

Figure (12) illustrates the translation of RMS noise into timing jitter. Figure (13) shows the model of an induced noise voltage generated due to radiated EMI. As shown in Figure (12), noise voltage (Δv) at zero crossing the signal v(t) to reach the threshold Δt earlier, thus produces jitter, The simplified expression of oscillator output containing extrinsic and intrinsic noise can be expressed by

$$v_0(t) = A\sin(\omega t) + v_n(t) \quad (9)$$

Where A is amplitude, ω is the angular frequency, and $v_n(t)$ is noise voltage at time t. The random noise $v_n(t)$ shows Gaussian distribution, the probability distribution $f(v_n)$ is

$$f(v_{int}) = \frac{1}{\sqrt{2\pi v_{int(RMS)}^2}} e^{-\left(\frac{v_{int}^2}{2v_{int(RMS)}^2}\right)} \quad (10)$$

The probability density as a function of the timing jitter Δt is evaluated by setting $v_n(t) = A \sin(2\pi f \Delta t)$

$$f(\Delta t) = \frac{1}{\sqrt{2\pi v_{n(RMS)}^2}} e^{-\left(\frac{A^2 \sin^2(2\pi f \Delta t)}{2v_{n(RMS)}^2}\right)} \quad (11)$$

From eqn. (11), for $\Delta t \to 0$, $\sin(2\pi f \Delta t) \cong 2\pi f \Delta t$, $f(v_n)$ is given by

$$f(\Delta t) = \frac{1}{\sqrt{2\pi v_{n(RMS)}^2}} e^{-\left(\frac{A^2(2\pi f \Delta t)^2}{2v_{n(RMS)}^2}\right)} \quad (12)$$

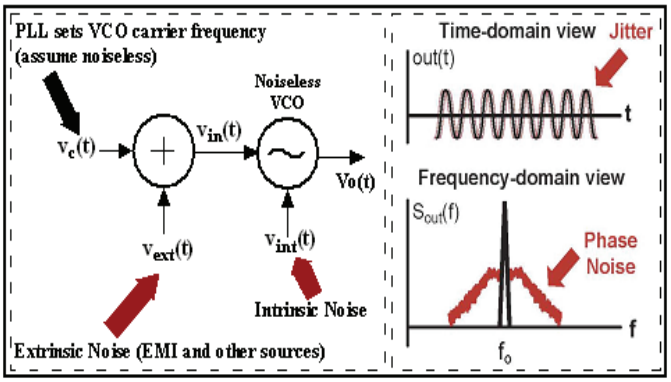

Fig. 11: Typical external noise sources (EMI and other noise sources) impacting oscillator noise dynamics

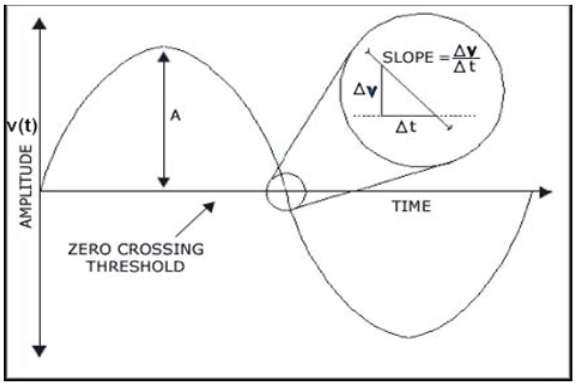

Fig.12. A typical noise voltage (Δv) at zero crossing the signal v(t) to reach the threshold Δt earlier, resulting timing jitter noise

Dividing the numerators and denominators terms of eqn. (12) by ($A\omega$) yields a jitter distribution function similar to the Gaussian distribution shown in eqn. (8), except for the scaling factor ($1/A\omega$):

$$f(\Delta t) = \frac{1}{A\omega}\frac{1}{\sqrt{2\pi \frac{v_{n(RMS)}^2}{A^2\omega^2}}} e^{-\left(\frac{\Delta t^2}{2\frac{v_{n(RMS)}^2}{A^2\omega^2}}\right)} \quad (13)$$

From eqn. (6) - eqn. (7), the root mean squares (RMS) jitter is given by

$$Jitter_{(RMS)} = \frac{v_{n(rms)}}{m_s} \quad (14)$$

Let Δt represents the jitter accumulated in one period (T_0),

$$\Delta t = \frac{T}{2\pi}[\phi(t_1) - \phi(t_2)] \quad (15)$$

Where T_0 is nominal period, t_1 is first zero crossing and t_2 is second zero crossing. From eqn. (15), the squared RMS jitter is

$$\left\langle \Delta t^2 \right\rangle = \left(\frac{T_0}{2\pi}\right)^2 \left[\left\langle \phi(t_1)^2 \right\rangle - 2\left\langle \phi(t_1)\phi(t_2) \right\rangle + \left\langle \phi(t_1)^2 \right\rangle\right] \quad (16)$$

Since $\phi(t)$ is stationary process:

$$\left\langle \phi(t_1)^2 \right\rangle = \left\langle \phi(t_1)^2 \right\rangle = \left\langle \phi(t)^2 \right\rangle$$

From Parseval's theorem:

$$\left\langle \phi(t_1)^2 \right\rangle = \left\langle \phi(t_1)^2 \right\rangle = \left\langle \phi(t)^2 \right\rangle = \int_{-\infty}^{\infty} S_\phi(f)df \quad (17)$$

$$\left\langle \phi(t_1) \times \phi(t_2) \right\rangle = R_\phi(t_2 - t_1) = R_\phi(\tau) \quad (18)$$

Where $S_\phi(f)$ is the spectral density of $\phi(t)$, and f is the offset (Fourier frequency), $R_\phi(\tau)$ is the autocorrelation function of $\phi(f)$ and $\tau \cong nT_0$ is the time after n^{th} period. The phase noise autocorrelation equals the cosine transform of the phase noise:

$$\text{Jitter}^2_{(RMS)}(\tau) = \Delta t^2_{RMS}(\tau) = \frac{2T_0^2}{\pi^2} \int_{f_L}^{f_U} £(f)[\sin^2(\pi f \tau)]df \quad (19)$$

$$\text{Jitter}_{(RMS)} = \sqrt{\Delta t^2_{RMS}} \quad (20)$$

Where f_L and f_U are the practical lower and upper frequency integration limits. In addition to EMI induced jitter, spurs also contribute to timing jitter, especially in oscillators caused by phase-locked-loop reference spurs, supply coupling, crosstalk from nearby circuitry, and sources. Therefore, each significant spur contribution should be accounted for separately as for the weighted k^{th} spur below:

$$\Delta\phi^2_{RMS\_k} = 8£(f_k) \times [\sin^2(\pi f_k \tau)] \quad (21)$$

$$\Delta t^2_{RMS}(\tau) = \frac{2T_0^2}{\pi^2} £(f_k) \times \sin^2(\pi f_k \tau) \quad (22)$$

$$\text{Jitter}^2_{RMS}(\tau) = \frac{T_0^2}{\pi^2} \sum_k £(f_k) \times \sin^2(\pi f_k \tau) \quad (23)$$

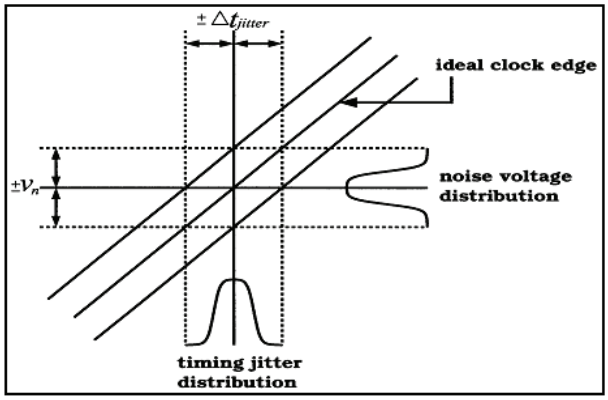

Fig. 13 An equivalent model of the EMI induced noise voltage [7]

Each spur's contribution (EMI, cross-talk, phase-locked-loop reference spurs, coupling and other sources) are then added in sum square fashion as follows:

$$\Delta t^2_{RMS\_Total} = \Delta t^2_{RMS\_EMI} + \Delta t^2_{RMS\_1} + \Delta t^2_{RMS\_i} + \cdots \Delta t^2_{RMS\_k} \quad (24)$$

$$\Delta t^2_{RMS\_Total} = \Delta t^2_{RMS\_EMI} + \sum_{i=1}^{k} (\Delta t^2_{RMS\_i}) \quad (25)$$

$$\text{Jitter}^2_{Total} = \text{Jitter}^2_{EMI} + \text{Jitter}^2_{Noise-Floor} + \text{Jitter}^2_{Phase-Noise} \quad (26)$$

From eqn. (1) - eqn. (26), radiated EMI induced noise voltage influences dynamically the operating resonant modes, transconductance and impedance transfer functions of the crystal oscillator circuit, resulting in induced sub-harmonic frequencies (lower than the fundamental frequency).

In addition to this, EMI induced noise voltage propagates through the circuit gates and this voltage can be amplified or reduced depending on the noise propagation path of the circuits, thus influences the time domain jitter dynamics. Many research works [1]-[17] have exploited different techniques to minimize the EMI by exploring novel crystal oscillator architectures. Although, research work [1-17] describes the efficient shielding to improve the EMI susceptibility and start-up dynamics of the crystal oscillator circuits but the associated circuitry requires large PCB area and not a cost-effective and power-efficient solution for an integrated reference frequency standard applications. In most systems, however, especially portable and handheld products, shielding becomes the least desirable method of EMI reduction. Shielding increases the size, weight, and cost; creating a substantial increase in labor costs, for example, because the shielding of these products is difficult to automate in manufacturing.

In this work, we report a novel circuit topology (Fig. 21) using dynamic phase-injection mechanism, including mode-coupling to avoid mode-jumping for low cost solution that minimizes the effect of EMI, while maintaining the high stability and phase noise performances.

IV. TEM Radiation and Minimization Techniques

A primary source of EMI radiation generated by an electronic circuit board during its active operation is commonly known as transverse electromagnetic mode (TEM) radiation. TEM radiation is generated mainly by the alternating clock current transmitted through the printed circuit board (PCB) traces, and the instantaneous current changes in the electronic board components. The TEM wave effect can account for up to about seventy five percent of the total EMI interference generated by the operating circuit board, and creates EMI radiation that is discharged from the edge periphery of the board substrate, which typically follows parabolic profile [18]. Furthermore, EM radiation can adversely affect circuit performance, and radiate from electronic equipment to threaten circuits in nearby equipment.

The simplified way is to suppress the noise interference by taking special care in routing signal to avoid EMI, but requires additional design time and often adding layers to the PCB. Ferrite beads, filters, and shielding were used to partially or completely mitigate the EMI problems. But these approaches are marginalized with the introduction of the phase-injection and spread spectrum clocking that suppresses EMI, including stability and jitter performance.

As system operating frequencies and the need for lower current consumption increases, physics dictates that end applications will also tend to become increasingly susceptible to externally generated EMI sources. These electrical influences can be generated by either radiated or conducted EMI noise sources. Radiated EMI noise sources include anything electrical or electromechanical, including motors,

power lines interference, antennas, traces on a Printed Circuit Board (PCB), and even the components on the PCB.

Conducted EMI noise sources primarily manifest themselves as electrical "noise" on the power supply lines of an application and can be caused by induced voltage spikes from external devices like those mentioned above, or by RF coupling within the system itself.

The CAD simulation techniques to predict conducted and radiated emission is a difficult and time-consuming task. It is a known fact that, during system development, critical signal-integrity and EMI (electromagnetic-interference) simulations are difficult, time-consuming, and error-prone due to their reliance on hard-to-predict models and parameter extractions. This situation worsens with every new product generation due to steadily increasing clock speeds and decreasing supply voltages, resulting in reduced noise margins [19,25].

In general, clocked digital devices generate electromagnetic emissions to some degree or another in the form of radiated or conducted RF energy. The current trend towards increasing operating frequencies aggravates the problem many folds by generating broader bandwidth RF noise. Ultimately, prevention of EMI related issues within a particular application remains the responsibility of systems designers.

Figure (14) shows the typical plot of the conductive EMI test using spectrum analyzer and impedance matched coupling network [20]. As shown in Figure (14), the conductive EMI test measures the noise that is directly coupled into the Vcc line to the crystal oscillator circuit.

It can be seen from Figure (14), amplitude of this noise is in tolerable limit for most of the consumer electronic products but this experiment is typical in nature and results can vary depending upon the shielding and other peripheral circuitry. As illustrated in Figure (14), one can notice that changing the resolution bandwidth increases the noise floor [20].

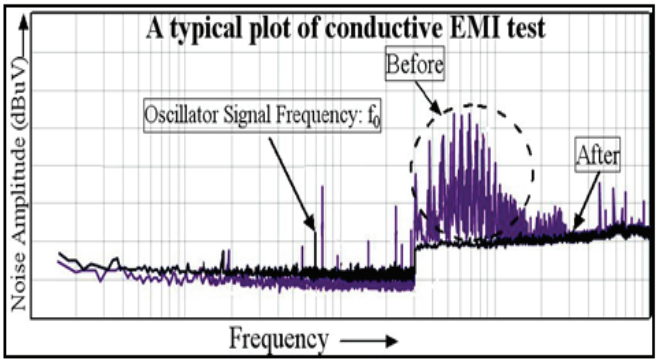

Fig 14: A typical plot of conductive EMI test [20]

Figure (15) shows the typical plot of the radiated EMI test, which shows the comparative insights about the radiated noise before and after noise suppression techniques (shielding and spread spectrum techniques). This typical radiated EMI test set up uses a spectrum analyzer, a wideband gain block, and a standardized test PCB for an evaluation.

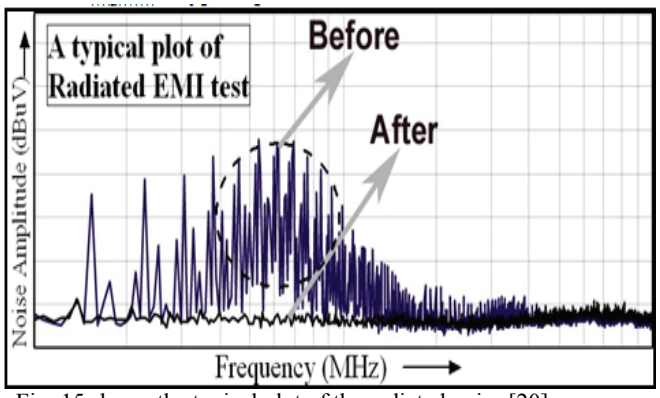

Fig: 15 shows the typical plot of the radiated noise [20]

An oscillator circuit is commonly significant source of radiated emissions in electronic systems. These emissions are often excited by the current flowing through the power-supply lead of the oscillator. Although seldom considered in circuit design, the spectrum of the large, periodic pulse of supply current drawn by an oscillator can occupy a wide bandwidth. As a result, substantial filtering with careful attention to return-current routing is often required to bring the emissions radiated from the supply lead into compliance.

The reported experiment measures the noise that could potentially be radiated into the crystal resonator surrounding electronic modules in the communication systems [20]. The measured conducted and radiated noise data as shown in Figures (14) and (15) is a typical qualitative representation and will vary based upon oscillator topology and the surrounding peripheral electronic circuitry and sub-systems.

V. Low EMI And Fast Start-Up Crystal Oscillator

The electromagnetic interference (EMI) is a complicated problem in the communication industry. Most of the communication systems rely on crystal oscillator as reference frequency standards for synthesis of the harmonic signal required for their operation. But mode-jumping phenomena of these reference sources limits the interference susceptibility that affects directly the system performance like, bit error rate (BER) in point-to-point radios, range and load capability of telephone networks, reliability of the navigation systems, and detection ability of radars etc.

This begins with the proper PCB layout and grounding, limiting trace lengths, placement of electrical components, and enclosure design. Again, selecting components at the outset, which offer low RF emissions and electrically robust characteristics, can only make the task easier and first pass success more likely. But, in practice, above techniques increases the real estate area and cost.

In this paper, we studied the circuit techniques based on phase-injection mechanism, which provides additional immunity towards EMI and jitter for the reference frequency standard applications. Experimental results and CAD simulated data provides insight into observed start-up and EMI dynamics, and validated with the design example of 100 MHz crystal oscillator circuit. For the high frequency operation, a method is needed to select a particular resonance mode so that other active modes such as: EMI-induced sub-harmonics, parasitic modes, and overtone modes fail to co-exist and sustained oscillations.

The simplified technique is to maximize the negative resistance generated from the active device network (Fig. 16) for a given particular mode and must yield positive value of resistance for unwanted modes, including EMI-induced oscillations. The value of the input impedance $Z_{in}(\omega)$ (looking into the base of the transistor in Fig .17) is given by

$$Z_{in}(\omega) \cong R_{in}(\omega) + jX_{in}(\omega) = -\left[\frac{Y_{21}}{\omega^2 C_1^* C_2}\right] + \frac{1}{j\omega}\left[\frac{1}{C_1^*} + \frac{1}{C_2}\right]$$

Therefore the negative resistance and resonator drive level at steady-state is described for circuit shown in Fig 16 as [13]

$$R_n(\omega) = -\left[\frac{Y_{21}(x)}{\omega^2 C_1^* C_2}\right] = \left[\frac{Y_{21}(x)}{\omega^2 (C_1 + C_{b'e}) C_2}\right] \quad (27)$$

$$I_R(\omega) \cong \frac{2I_E(\omega)}{\omega C_2 R_n(\omega)} \quad (28)$$

Where

$$Y_{21} = G_m(x) = \frac{qI_{dc}}{kTx}\left[\frac{2I_1(x)}{I_0(x)}\right]_{x=\frac{g_m I_R(\omega)}{\omega(C_1+C_{b'e})I_E(\omega)}} \quad (29)$$

$I_1(x)$ and $I_2(x)$ are the modified Bessel functions of order 0 and 1 respectively. From eqn. (14) and eqn. (15), resonator current drive level $I_R(\omega)$ can be lowered by increasing the value of feedback capacitor C_2 (Fig. 17) for a given current $I_E(\omega)$ but at the cost of reduction in the value of negative resistance $R_n(\omega)$.

In order to maintain the same value of negative resistance $R_n(\omega)$ as required to compensate the loss resistance of the crystal resonator at steady-state oscillation, the value of the feedback capacitor C_1 (Fig. 16) has to be reduced. But there is a practical limitation of the minimum value of the C_1, which is to be decided by a specified value of the load capacitance of the crystal resonator, including the intrinsic base-emitter capacitor ($C_{b'e}$) of the transistor (Fig.16) [4]-[6]. Moreover, drive-level parameter determines the overall nonlinearity, which causes amplitude-frequency effect, and degrades the 1/*f* noise performances [10].

In this paper we describe drive-level optimization techniques to enable high frequency operation (without witnessing breakdown phenomena of the crystal resonator in UHF/VHF frequency range). This can be accomplished by using mode-coupling technique (tuning the L_m-C_m at higher order modes) and optimizing the ratio C_{V2}/C_{V1} for reducing the start-up time (time interval required for an oscillator to sustain stable output at desired frequency) and drive-level (Fig.17).

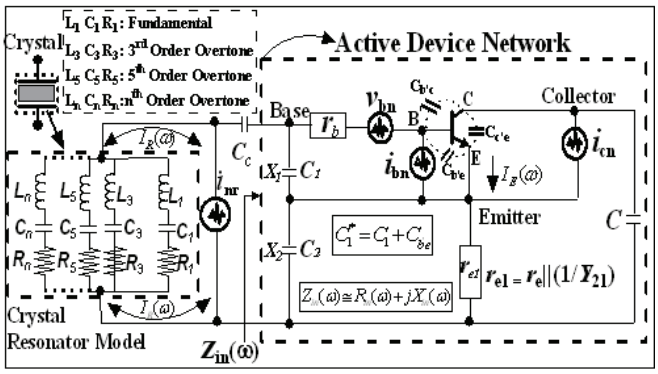

Fig.16: A simplified crystal oscillator including noise contributions.

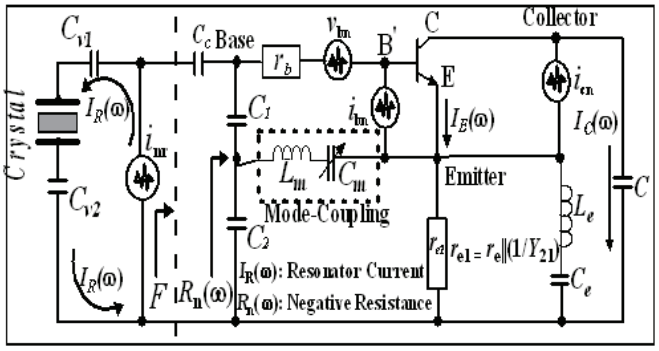

Fig.17: A typical crystal oscillator including noise contributions.

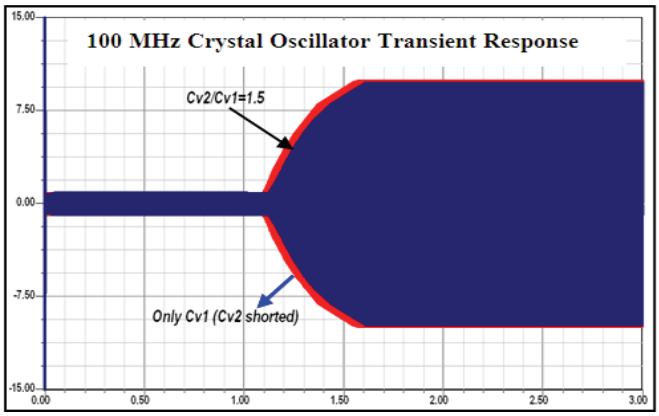

Fig.18: Simulated plots of the start-up dynamics for a given IR(ω)

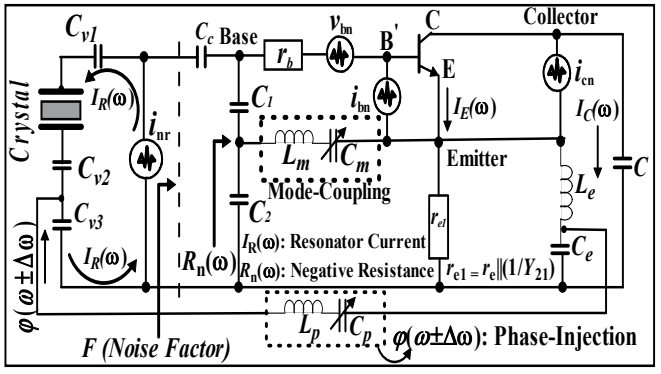

Fig. 19: A typical mode-coupled phase-injected φ(ω±Δω) crystal oscillator, including noise contributions (transistor and resonator)

Figure (18) shows the simulated plots of the start-up characteristics (for a given C_{I2}/C_{V1}=1.5 and C_{I2} shorted), we found that there is a trend in reduction of the start-up time provided we optimize the ratio of the coupling capacitors C_{V1} and C_{V2} for a given drive-level $I_R(\omega)$.

However, the reduction in the start-up time is not appreciable and limited to 2-5% (Fig 10, C_{I2}/C_{V1}=1.5) for a given drive-level $I_R(\omega)$. Further reduction in start-up time can be achieved by phase-injection $\varphi(\omega\pm\Delta\omega)$ mechanism for a given mode-coupling and the drive-level $I_R(\omega)$ (Fig. 19).

In general, coupling capacitor C_{V1} suffice the oscillation growth (without C_{I2} and C_{V3}) but at the cost of slow start-up characteristics and high drive level $I_R(\omega)$. Figure (20) shows the simulated plots of the star-up characteristics (for a given C_{I2}/C_{V1}=1.5, C_{I3}=10 pF; C_{I2}/C_{V1}=1.2, C_{I3}=10 pF; C_{I2}/C_{V1}=1, C_{I3}=10 pF) for 100 MHz crystal oscillator circuit (Fig. 21).

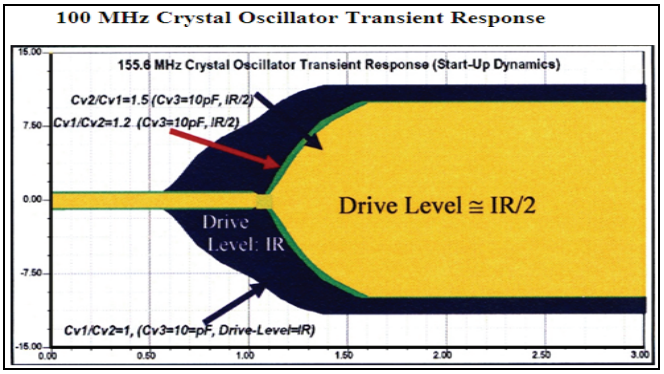

Fig.20: Simulated plots of the start-up dynamics for a scaled IR(ω)

It is obvious from the Figure (20) that phase-injection network improves the start-up dynamics for a given coupling ratio of C_{I2}/C_{V1}=1.5, and C_{I3}=10 pF, including reduction of 50 % drive-level current ($\cong I_R/2$).

Figure (21) shows the typical schematic of the mode-coupled phase-injection locked 100 MHz crystal oscillator (XO) circuit, which sets up optimum and noise impedance transfer function by dynamically controlling mode-coupling and phase-injection for a given drive level and star-up time.

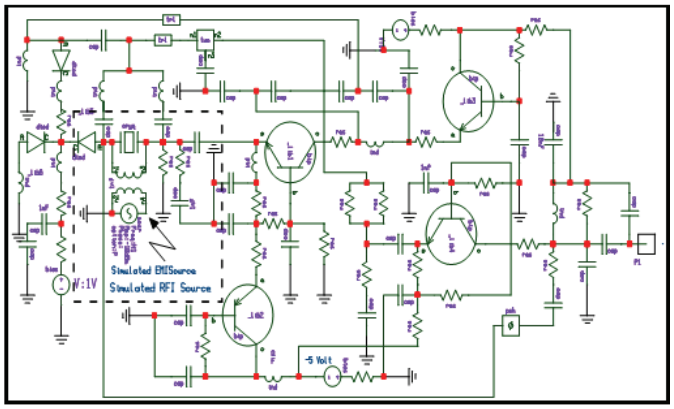

Fig. 21: Schematic of 100 MHz mode-coupled Crystal oscillator

As shown in Figure (21), the higher order mode is coupled through output path and feedback to the point where frequency-drive sensitivity of the crystal resonator shows maximum group delay and faster slew rate, resulting, improved EMI performance with reduced drive-level $I_R(\omega)$.

Figure (22) shows the CAD simulated phase noise plot, for without and with mode-feedback mechanism. The circuit operates at 5V, 20 mA and also suitable for tunable crystal oscillator for VCXO (voltage controlled crystal oscillator) applications.

The biggest challenge is the characterization of EMI simulated interference sources for the validation of EMI-induced failure due to frequency shift caused by induction of sub-harmonics into crystal resonator. In addition to this, phase-injection locking mechanism is very critical, slight variation in phase may cause oscillation to cease; therefore, phase-locked-loop (PLL) option can be more practical for commercial applications.

Although, mode-coupling phase-injection restricts the frequency drift to the greater extents still crystal oscillator can induce sub-harmonic response under the influence of external radio frequency interference (RFI) around the crystal oscillator circuit.

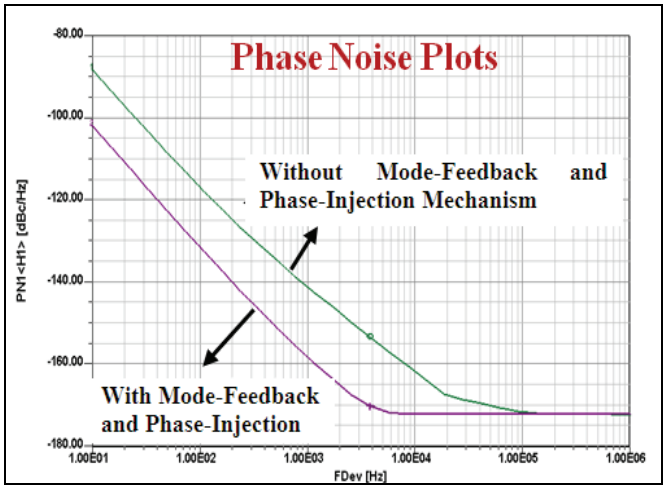

Fig. 22: Simulated phase noise plot of crystal oscillator

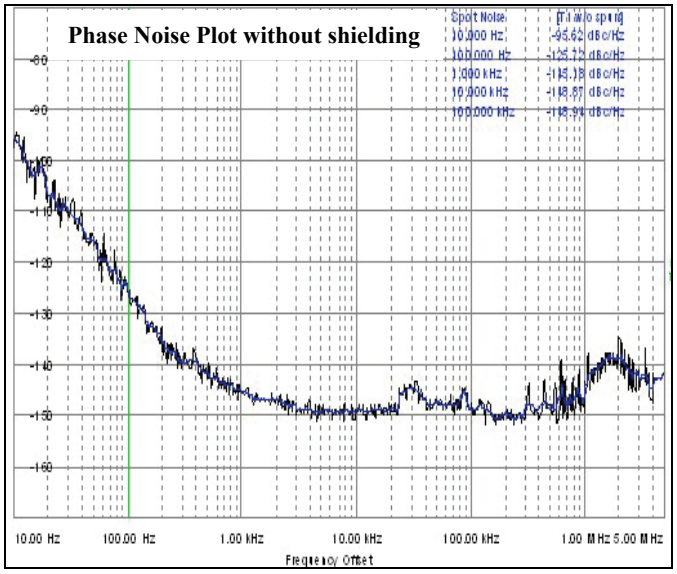

Fig. 23: Measured phase noise plot of 100MHz XO without shielding

Figures (23), (24) and (25) shows the measured phase noise plot of the 100 MHz crystal oscillator circuit using without shielding, with shielding, and with mode-feedback mechanism. By proper shielding and making arrangement of mode-feedback network, including EMI insensitive traces for power and ground line can improve jitter and the stability against EMI-induced failure.

As illustrated in Figures (23), (24) and (25) the novel phase-injection mode-feedback techniques improves the stability and phase noise performance by 10-15 dB. The circuit operates at 5V, 30mA and suitable for tunable crystal oscillator applications.

Another example of 155.6 MHz mode-coupled and phase-injected crystal oscillator for the validation of the details was studied where external interference is characterized by RF pulse (single and multiple pulses) source inductively coupled with the crystal lead inductance. Figure (26) shows schematic of 155.6 MHz XO under the influence of EMI.

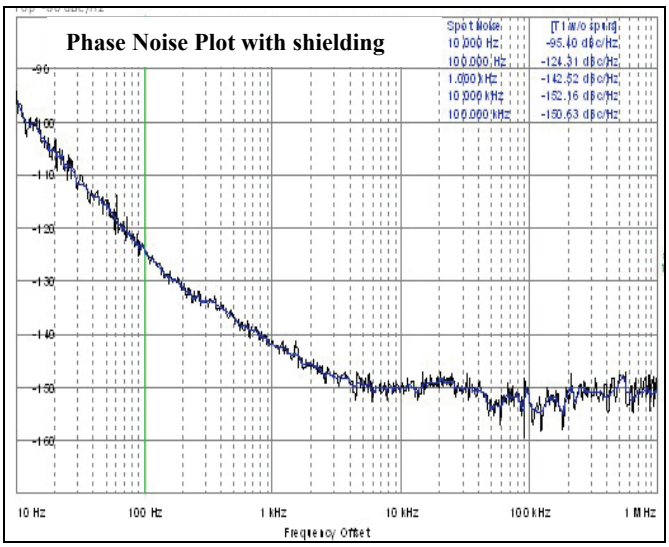

Fig. 24: Measured phase noise plot of 100MHz XO with shielding

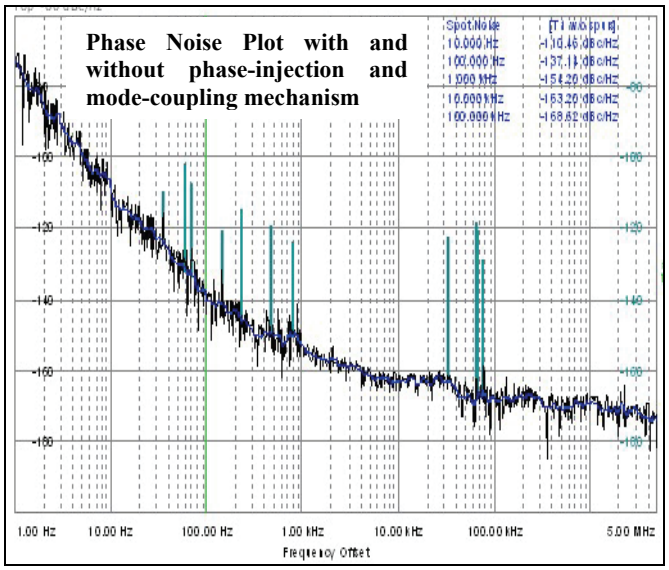

Fig. 25: Measured phase noise plot of 100MHz XO with phase-injection and mode-feedback mechanism.

This exercise gives the qualitative insights about the EMI sensitiveness of the crystal oscillator circuit and emphasizes the fact that crystal resonator is intrinsically sensitive to EMI failures. And, this effect (shift in frequency) is more prone at high frequency (UHF/VHF) range and it affects dynamic range, selectivity, and sensitivity of a receiver. Therefore, designing a low cost EMI-insensitive crystal oscillator circuit at high frequency (UHF/VHF) is challenging task when the circuit is temporarily exposed to continuous or pulsed RF electromagnetic fields, which creates hysteresis (the new state persist even after the RFI source is removed) and leads to hang-up in digital system [1]. Figures (27), (28) and (29) show the frequency shift, schematic and phase noise plots of 155.6 MHz XO under the influence of EMI.

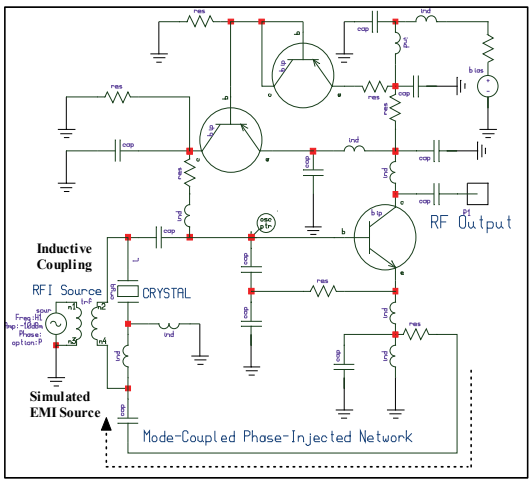

Fig. 26: A typical 155.6 MHz mode-coupled phase-injected crystal oscillator with external coupled RF pulse source (inductive coupled)

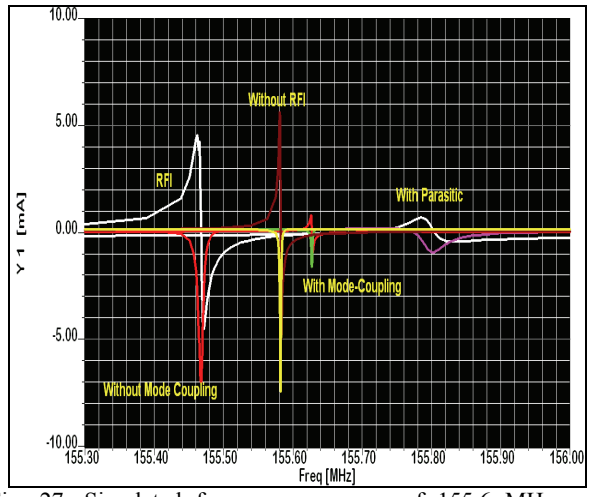

Fig. 27: Simulated frequency response of 155.6 MHz crystal oscillator in the presence of coupled interference source as shown in Fig. (26)

The likelihood of frequency shift in a noisy EM environment is far higher, however, this paper describes the mode-coupled phase-injected techniques to restrict the shift up to acceptable degree due to radiated EMI (as shown in Fig. 27) and also minimizes the phase noise by 8-10 dB (Fig. 29).The mode-coupled phase-injection approach minimizes the mode-jumping and phase noise due to radiated EMI

(validated using loop antenna induced by continuous wave EMI).

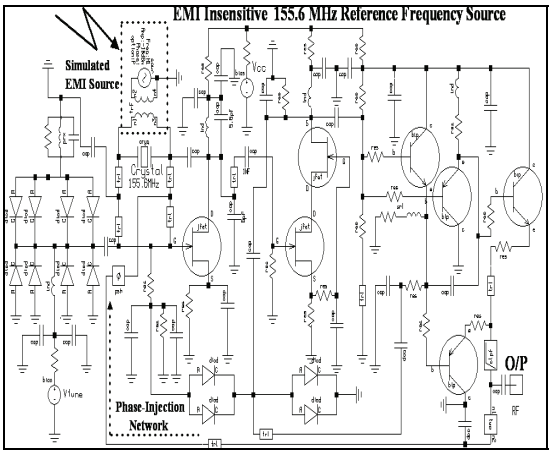

Fig. 28: A circuit schematic of EMI insensitive 155.6 MHz XO

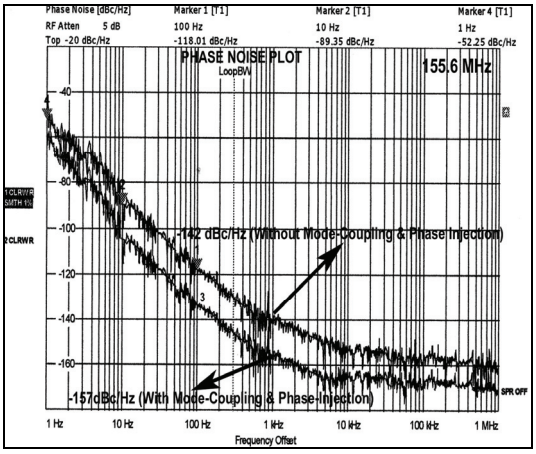

Fig. 29 The measured phase noise plot of 155.6 MHz XO (for the schematic in Fig. 28)

VI. CONCLUSION

Modern communication systems are particularly susceptible to electromagnetic interference (EMI), which can induce the crystal oscillator circuits to oscillate at different modes and sub-harmonics. As a by-product of a normal mode of operation, start-up dynamics and stability also deteriorates under the influence of electromagnetic radiation/interference. This work offers a novel crystal oscillator circuit using mode-coupling and phase-injection techniques for improved electromagnetic interference (EMI), start-up, and drive-level, dynamics for the realization of high frequency reference frequency standards.

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