Simple Modelling Approach for Via-Hole Characterization on Silicon Substrate at Ka-Band

K. Singh, K. Nagachenchaiah

Abstract **– This work presents a simple model of via-hole using electromagnetic field solver. Equivalent model parameters on Si are found out at Ka-band. Proposed single via-hole model has been compared with theoretical published data. The effect of via-hole radius and substrate height at Ka-band frequencies has been studied. Further, S-parameter analysis and comparison for multiple vias at two different frequency bands is carried out.**

Keywords **– Via-hole, radio-frequency, high resistivity substrate, conductor backed- CPW (CB-CPW), grounding.**

I. INTRODUCTION

Silicon based CMOS technology has proved to be a cost-effective process for the development of advanced radio frequency and mixed signal integrated circuits where interconnections and grounding play a very prominent role. Vias are used in single layer, multilayer PCBs and RFICs to provide ground paths or connect various layers. Planar transmission lines like microstrip and CB-CPW lines are used not only for packaging and mounting reasons but also to reduce the overall size of the substrate as they can be easily mounted on a metallic carrier due to backside metallization. Generally the broadband circuit grounding (including DC ground) can be realized by through substrate via holes, wrap around metallization or bond-wires. Via-hole process helps in realization of improved electrical performance and miniaturization. Otherwise, a topside metallization pattern near the periphery of the chip is used for connecting the backside ground or metallic carrier requires additional crossovers, more surface area and introduces additional parasitics. As the operating frequency increases, an accurate, simple and scaleable model of via becomes a fundamental and dominant requirement. Moreover in CMOS and MEMS based RF circuits; via-holes are an established technology for grounding and short circuiting planar transmission lines. At radio frequencies, short circuit can also be implemented by a quarter-wavelength open-circuited stubs. This causes complete phase reversal at the desired frequency due to line length resulting in zero impedance at the reference plane. As the frequency increases or decreases, finite reactance of the stub results in appreciable change of impedances; resulting in degraded performance. To circumvent this phenomena via topology is preferred which additionally helps in elimination of radiation losses.

Often, via is modelled as a frequency independent inductance [1]. Earlier work [2] demonstrated an analytical model for a single via where inductance variation due to substrate height and thickness was included. The empirical formula proposed [3] also model inductance variation with varying via-diameter and substrate height. Advanced model proposed by Swanson et al [4] shows capacitance effect due to pad width variation. P.Kok [5] et al used intro-differential equations to extract excessive capacitance and inductance utilizing commercial 3-D electromagnetic simulator. The work reported by Strohm et al [6] modelled ground via as inductance is applicable only up to certain frequencies. At higher frequencies, parasitic resistance due to radiation and capacitance also becomes an important factor in predicting the circuit performance which is not considered in the works reported thus far.

This article proposes a simple and easier modelling approach for finding the lumped element equivalence from field-solver generated data which can directly be incorporated in circuit simulators. To obtain realistic data, S-parameter approach is utilized instead of Z-approach to account for reference plane effects on the derived parameters.

Kamaljeet Singh and K.Nagachenchaiah are with Semi-Conductor Laboratory, Near Chandigarh,India, E-mail: kamaljs@scl.gov.in

II. SINGLE-VIA MODEL

A single via-hole and its equivalence in microstrip is shown in Fig. 1. Equivalence shows parasitic radiation resistance (R_s) associated with frequency dependent inductance (L) in series along with shunt capacitance (C) resulting from top and bottom metallization. R_t is the equivalent resistance associated with the via-hole inductance.

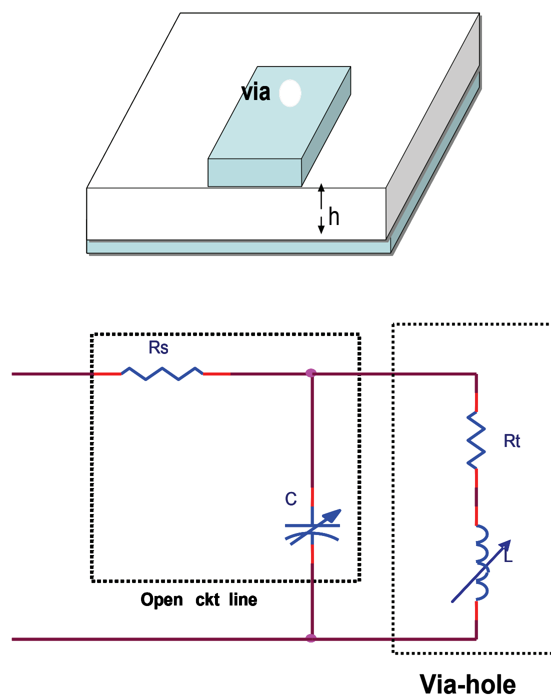


Fig. 1. Single via and proposed equivalence

The study is carried out taking high resistivity silicon (ρ=8K ohm-cm) having substrate height h=270µm. Theoretical equivalence of open circuited line (< λ/4) can be modelled as combination of resistor-capacitor as shown in Fig.2 where Z_0 is the characteristics impedance of line (50Ω). The approach is based on basic lumped capacitor behaviour of open circuit line and resistive part (Rs) represents losses associated with thin film metallization. The equivalent values are extracted from the impedance characteristics. The equivalent capacitor at various frequencies can be found out using MoM based field solver in the 10-35 GHz range for 50Ω input impedance.

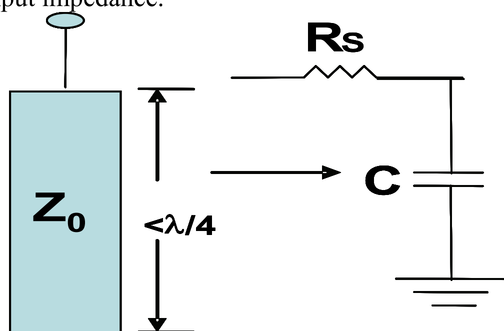


Fig. 2. Open-circuited transmission line and its equivalence

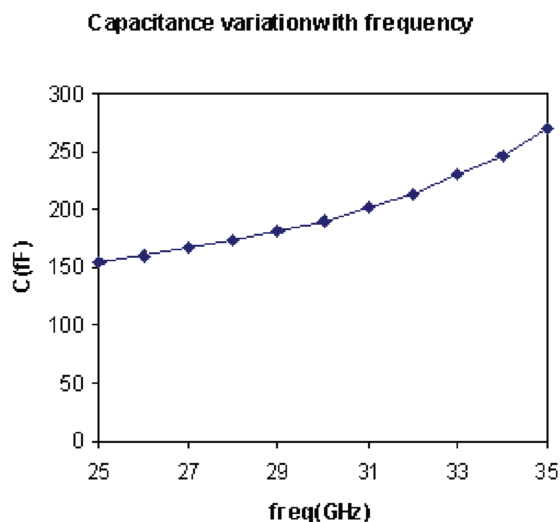


Fig. 3 Variation of capacitance with frequency

Fig. 3 shows the parabolic behaviour of capacitance which is fitted in 25-35 GHz range and given in equation 1.

$$C\ (f\,F) = 0.8774\, f^{2} - 41.707\, f + 651.77 \qquad (1)$$

where f is frequency in GHz. The appreciable change in the reactance is due to the introduction of the line at frequencies other than quarter-wavelength.

III. EXTRACTING MODEL PARAMETERS

The open-circuited stub shown in Fig 2 is modified by inserting via as depicted in Fig. 1. The via introduces inductance, as is well reported, and the empirical model as proposed is [4]

$$L_{via} = \frac{\mu_0}{2\Pi}\left[h \ln\left(\frac{h+\sqrt{r^2+h^2}}{r} \right) + \frac{3}{2}\left(r - \sqrt{r^2+h^2} \right) \right] \qquad (2)$$

where r is the radius of the via-hole and h is the height of the substrate.

Full wave predicted inductance L is computed and plotted along with the inductance values obtained from equation (2) in Fig. 4. It is seen that inductance varies by about 50 % from theoretical value. This difference could be attributed to limitations of the theoretical model as it does not account for finite resistivity and thin film metallization effects associated with parasitics at higher frequencies. Radiation resistance R_t associated with L is also derived from the full wave predicted value These values are extracted for silicon substrate of height 270µm at 30 GHz.

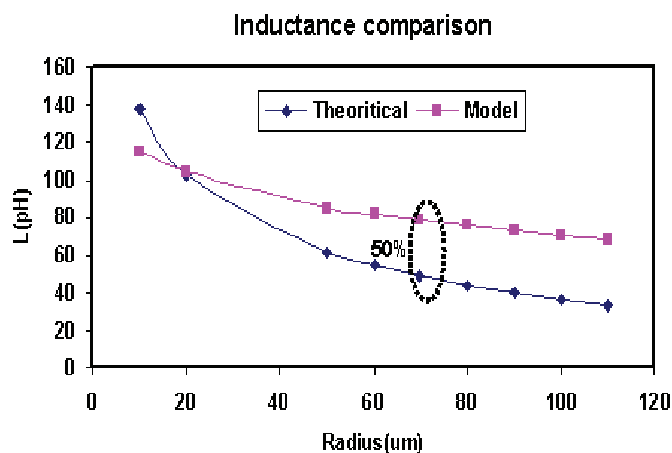
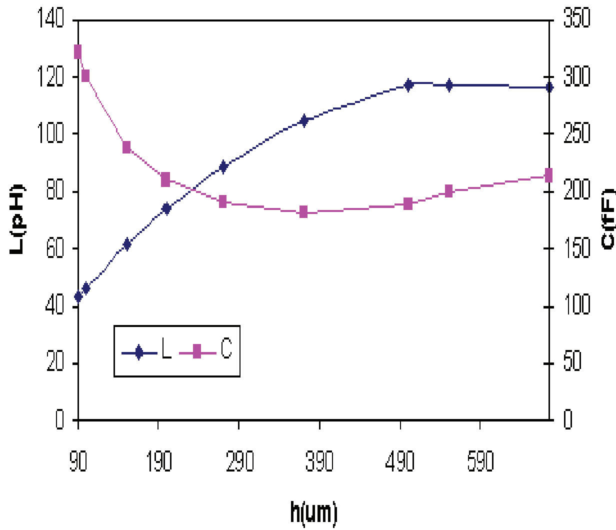


Fig. 4 Inductance and resistance variation with changed radius

As can be seen inductance decreases with via radius as ground paths for current are shortened.

Effect of varied substrate height on the parameters is also found out. Keeping the frequency (30 GHz) and via radius (50µm) constant, effect of substrate height on inductance and capacitance is plotted as shown in Fig. 5. Plot shows difference in theoretical formulation and full wave simulated results as theoretical model doesn't accounted frequency and resistivity impact.

Substrate height plays an important role as increased height introduces extra current path resulting in high inductance value. Capacitance value varied with changed substrate height 'h' and its value decreases with increased gap (h). Fig. 6 shows frequency dependent variation of inductance and capacitance with via radii. These parameters are more sensitive at smaller hole diameters compared to larger vias. It can be seen from the plot that capacitance increases with frequency whereas inductance is more sensitive to via radius at lower frequencies and its radii effect on inductance is minimal at higher frequencies.



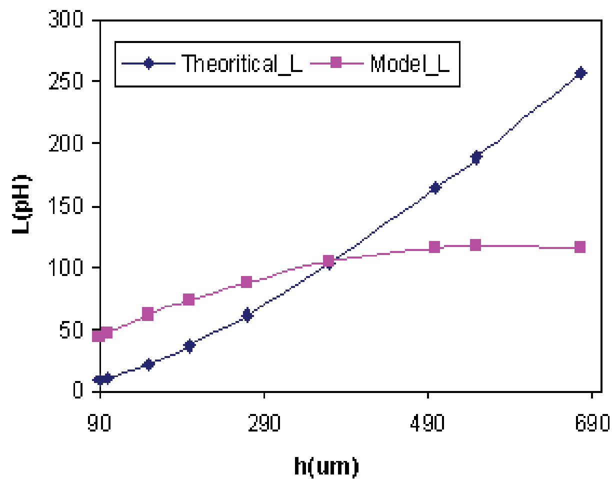


Fig. 5. Inductance and capacitance variation with substrate height

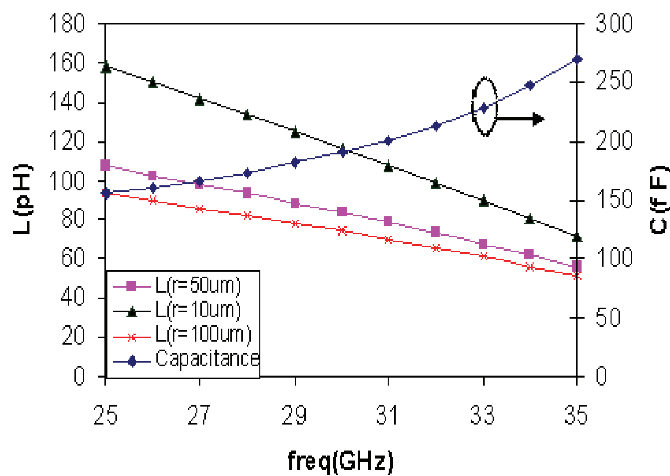


Fig. 6. Parameters variation with frequency

IV. Role of Vias on Circuit Performance

The number and distribution of vias play an important role in determining the circuit performance in particular frequency band. A comparative study of losses is carried out at Ku and Ka-bands with respect to number of vias. Finite ground-CBCPW transmission line is chosen due to its wide bandwidth starting from DC and ease of implementation in silicon based radio frequency integrated circuits (RFICs). Further, as shown in Fig. 7, it suppresses unwanted modes.

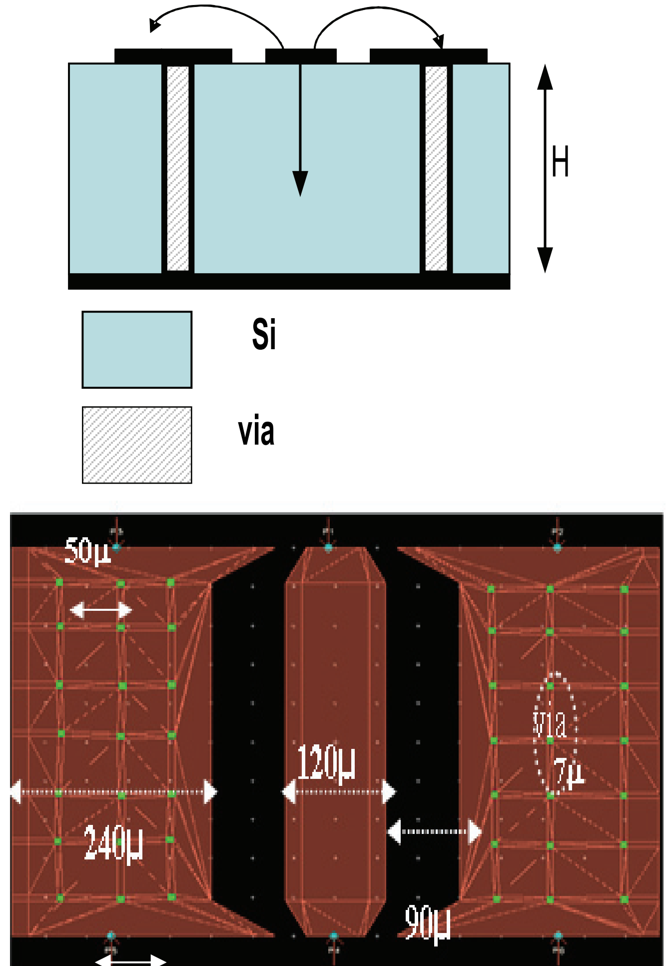


Fig. 7. Schematic of via-hole topology

The simulation results carried out on 500 µm, CB-CPW line having 7 µm vias, are shown in Fig. 8. The study indicates that at Ku-band (17 GHz), the losses are not affected by the insertion of vias beyond two. But at Ka-band (30 GHz), the losses are increased due to series resistance Rs and higher radiation associated at higher frequencies. The reduction of overall resistance, caused by the paralleling of resistive component of vias, improves the insertion loss in the 12-24 via region whereas the return loss is not affected with the insertion of multiple vias. This effect can be mitigated by employing non-uniform vias and spacing but at the expense of fabrication complexity and circuit fragility. Judicious choice of selecting the number of vias is essentially a compromise between circuit performance and ease of implementation.

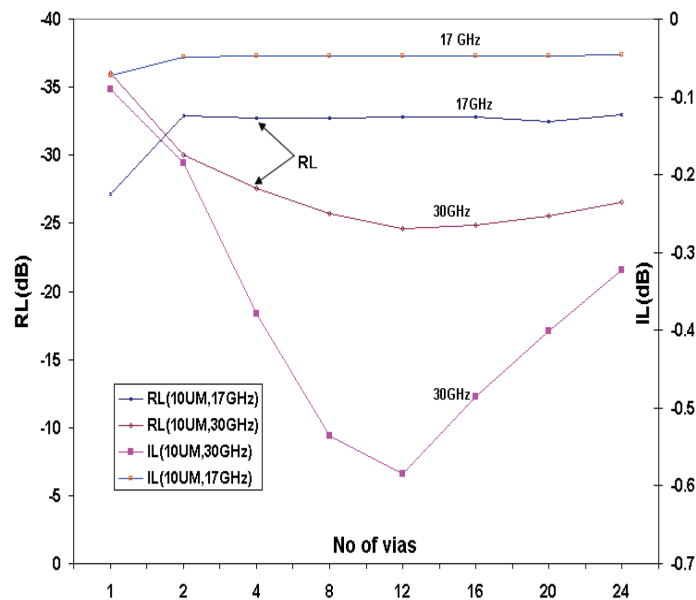


Fig. 8 Effect of vias on CB-CPW line characteristics

V. CONCLUSION

In this article, a lumped scalable equivalent circuit via-model fitted with field-solver geometrical data on silicon is presented. A design approach of via structure without resorting to hardware fabrication and characterization is also demonstrated. Proposed model can be scaled to take into account frequency dependent behaviour of generated lumped via-parameters. It may be noted that the values generated are for fixed resistivity and will partially change with resistivity variations. The geometry proposed can be useful for electrical through wafer interconnects thereby enabling 3-D structures for MEMS and ICs as well as permitting new packaging and integration geometries. Authors believe that this model will be useful in silicon based millimetric wave circuits because of its simpler implementation in circuit level simulators.

ACKNOWLEDGEMENT

Authors wish to thank Mr Ayan Karmakar for his support in this analysis.

REFERENCES

[1] E. Holtzman, *Essentials of RF & microwave grounding, Artech House*, 2006

[2] D. G. Swanson,” Grounding microstrip lines with via-holes,”*IEEE Trans on Microwave Theory and Techniques*, Vol. 40,No. 8,August 1992, pp. 1719-1721

[3] D. G. Swanson, W.T.R Hoefer, *Microwave circuit modeling using electro-magnetic field simulations*, Artech House 2003.

[4] M. E. Goldfarb, R. A. Pucel, ”Modeling Via Hole Grounds in Microstrip,” *IEEE Microwave and Guided Wave Letters*, vol. 1, no. 6, June 1991,pp 135-137

[5] P. Kok and D. De Zutter, ”Capacitance of a circular symmetric model of a via hole including finite ground plane thickness,” *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 1229-1234, July 1991

[6] K. M Strohm, P. Nuechler, C. N. Rheinfelder, R. Guehl, "Via Hole technology for microstrip TL & passive elements on high resistivity Silicon," *IEEE MTT-S Digest* 1999, pp. 581 - 584.