Hybrid DDS-PLL HF Frequency Synthesizer for FH-SS Radio

Igor S. Šajić, Jugoslav J. Joković[1], Slavko D. Šajić[2]

Abstract – **A proposal for the complete suppression of spurs arising from cutting off the phase in the direct digital frequency synthesis phase accumulator is implemented and tested. The Frequency Hopping Spread Spectrum (FH-SS) frequency synthesizer scheme is proposed for generating RF carrier in the HF band. The synthesizer was realized by combining Direct Digital Frequency Synthesis (DDFS or DDS) and Phase Locked Loop (PLL). In order to illustrate performance of the proposed scheme,corresponding measurements were performed.**

Keywords – **Modulation, Reference clock, PLL, DDS, Synthesizer.**

I. INTRODUCTION

Generating carrier signals is of paramount importance in radio communication systems. The performance of this signal defines the basic characteristics of the radio transmitters, such as the spectral purity of the output signal, the phase noise of the transmitter, the stability and output frequency resolution, etc. The requirements regarding carrier frequency in agile radio-communication systems (FH-SS) are additionally complex when the synthesizer is realized. In addition, there is a requirement for a rapid change in the frequency of the carrier. The most commonly used technique for generating a carrier is the phase synthesis based on the Phase Locked Loop (PLL). The PLL-based frequency synthesizer isnot complex, providing a relatively wide range of frequencies that could be generated and a good suppression of parasitic signals comparing to the level of the useful signal. The main disadvantages are the inability to achieve a high resolution and a relatively long time of switching from one frequency to another [1].

Another widely used technique is Direct Digital Frequency Synthesis (DDS), which is increasingly used in modern radio-communication systems, alone or in combination with PLL. Since DDS isbased on digital operations, it is possible to achieve a very rapid change in output frequencies, which is especially important with the Frequency Hopping Spread Spectrum (FH-SS) system. In addition, the DDS provide a large output resolution, low phase noise, a high ratio of minimum and maximum output frequency, the ability to perform all types of digital modulations, continuous linear change of output frequency, etc [2].

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However, in comparison with PLL synthesis, DDS has a limited range of output frequency and higher level of parasitic (undesirable) spectral components. Since the level of spurs in the DDS output signal is unacceptable in most RF wireless applications, the direct use of DDS to generate carrier signals in the transmitter is not appropriate. The situation is worse in the case of radio transmitters with non-linear amplifiers.

The realization of agile synthesizers in the HF band (2-30 MHz) is additionally complex because the Voltage-Controlled Oscillator (VCO) that should to "cover" the frequency range consisting of four octaves. Therefore, in order to cover the HF band with one VCO, the ratio of the capacitance of the varicap diode $C_{vmax}/C_{vmin} = 225$ is required, which today's technology does not support. In this case, it is necessary to realize a number of VCOs that would be switched on depending on the desired frequency. However, in FH-SS systems where fast switching from one frequency to another is required, the use of multiple oscillators depending on the desired frequency is not an acceptable solution due to the relatively long oscillator stabilization time after it is switched on. On the other hand, the simultaneous operation of more VCOs creates difficulties to ensure their mutual isolation to achieve the spectral purity of the output signal.

Bearing in mind the previously mentioned problems of generating carrier frequencies in the FH-SS systems of the HF band, and using the advantages provided separately by PLL and DDS, the hybrid FH-SS synthesizer for generating carrier frequencies in the HF band is proposed, implemented and analysed.First, a brief overview of the source of undesired signals in the DDS is given, as well as the proposal of their suppression. Also, a block diagram of the hybrid synthesizer for generating RF carrier signals in the HF band is proposed and described. Finally, the results of the measurements are shown, together with the corresponding conclusions.

II. PROPOSED DESIGN

A. Suppression of Spurs due to Phase Shortening in DDS

As said, one of the basic disadvantages of DDS is its spectral impurity. In a DDS there are several sources of undesired spectral components, two of which are the most important. The first source is the resolution of the Digital to AnalogConverter (DAC), which leads to an error due to the quantization of the sine wave signal. In the frequency domain, quantization errorsappear as discrete spectral components at the DAC output. Increasing the DAC resolution reduces the quantization error and, therefore, the level of unwanted spectral components in the reconstructed sine wave. The ratio of the useful signal powerto the quantum noise is determined as SQR = 1.76 + 6n (dB), where n represents the number of bits in the resolution of the DAC.

The second source of the spurs is caused by the shortening of the word of the phase accumulator. Namely, if the length of the word in the phase accumulator is *A*, only *P* higher bits are used in the phase amplitude conversion. Apparently, phase errors that are introduced by shortening the accumulator will cause errors in the amplitudes during the process of phase conversion into amplitude of the DDS. These errors are periodic and regardless of the selected word for setting the output frequency, after a certain time the accumulator phase and the shortened phase will match. Since these amplitude errors are periodic in the time domain, they appear as spectral lines in the frequency domain (known as phase truncation spurs). Fig. 1 shows the *A*-bit phase accumulator. The higher *P* bits are the phase words (bits used for the phase-amplitude conversion). As for phase resolution, lower *A-P* bits are truncated. The tuning word, *T*, consists of *A-1* least significant bits. It can be shown that the size and distribution of phase truncation spurs depends on: accumulator length (*A* bits), phase word size (*P* bits); that is number of phase bits after truncation, as well as size of setup word (*T*). A precise analysis of truncation spurs distribution is complex [3], [4]. Some practical methods for calculating the location and amplitude of the spurs in relation to different DDS parameters are given in [5].

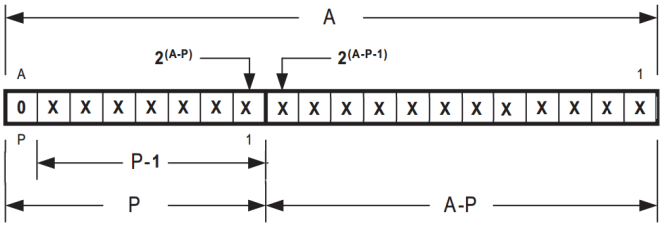


Fig. 1. Phase accumulator

The tuning words that give the maximum level of spurs are those that satisfy the following: GCD (T, 2^{A-P}) = 2^{A-P-1}, where GCD (X,Y) is the greatest common divisor of X and Y. Any tuning word with 1 at position 2^{A-P-1} and 0 in all less significant positions will give the worst level of spurs due to phase shortening (Fig. 1). On the other hand, there are setup words that do not lead to phase shortening, and they do not generate phase truncation spurs. Such tuning words must satisfy GCD (T, 2^{A-P}) = 2^{A-P}. Any tuning words that do not meet the previous condition will cause spurs due to phase shortening.

Phase dithering can reduce the energy of the spurs; however, it is paid by increased noisepower and by increased the phase noise. Previous research related to phase shortening spurs generally provided some improvements with the degradation of some other characteristics [6-8].

Based on the previous analysis, it can be concluded that the words *T* that cause spurs due to shortening of the phase give a non-integer ratio of the input and output frequencies, (F_S/F_0). In the case when an integer ratio (F_S/F_0) is provided for any frequency from the DDS generating range, the effects due to phase shortening could be avoid. In this case, the word *T* would have all zero at (*A-P*) lower positions in the phase accumulator. On this way, the spurs due to phase shorteningare completely suppressed in the output signal. In order to avoid spurs due to phase shortening of the, we proposevariable the reference frequency of the DDS, calculated as:

$$F_S=F_0*2^A/T_{int}, \quad (1)$$

where: *A* is length of the accumulator, T_{int} is the integer word for tuning the frequency defined by the (*P-1*) bits of Fig. 1, where the remaining (*A-P*) bits are always zero. From expression (1) we can conclude that the output frequency can be generated for different input frequency values, depending on the word T_{int}, meaning that the ratio of the maximum and minimum frequency at the input and output does not have to be the same.

The question arises, how to generate a variable reference (system) frequency that will provide aninteger ratio of reference and output frequency, in order to ensure high spectral purity, while keep all the advantages of DDS. We propose a solution to this problem through the realization of the agile synthesizer of RF carrier frequencies in the HF band.

B. Model of HF/ FHSS Synthesizer

The block diagram of the proposed FH-SS/HF frequency synthesizer is given in Fig. 2. The proposed scheme uses two DDSs. The first DDS-1 is triggered by a fixed frequency F_C, and provides a reference signal F_R for a phase loop that generates signals in the VHF band (60-90 MHz). The PLL output signal provides for DDS-2 a variable reference frequency F_S, which is the integer of the output HF frequency. For each output frequency F_0, the word for tuning (Tuning word-2) is selected so that the input frequency F_S is an integer of F_0. Also, realized VHF band contains any frequency from the HF band multiplied by the integervalue. In this way, we secured the suppression of spurs caused by phase shortening.

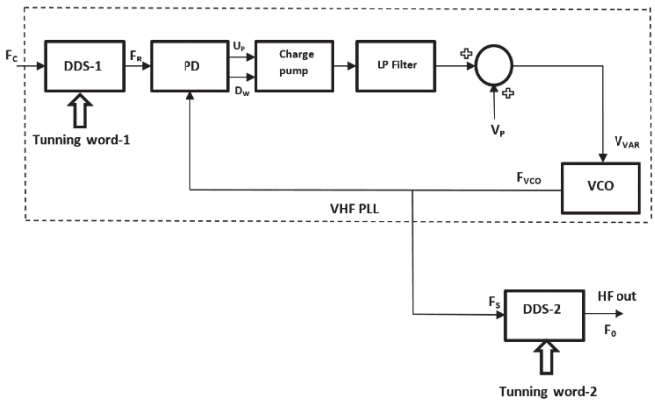


Fig. 2. Block diagram of the FH-SS/HF frequency synthesizer

The proposed PLL configuration uses a "unit" phase loop without multiplying the reference frequency, F_R. The output frequency of the PLL (F_{VCO}= F_S) is equal to the reference frequency F_R, so the unit loop acts as a narrowband filter at the reference frequency F_R. The width of the band around F_R defines the parameters of the PLL, the natural frequency ω_n and the damping factor ξ. In the output signal spectrum (F_{VCO}), the phase loop will suppress parasitic spectral components located outside the bandwidth of the PLL. In this

way, the broadband parasitic components and components due to phase shortening, which are present in the reference signal F_R generated by DDS-1 are suppressed. Changing the output frequency of the PLL is done by changing the frequency of DDS-1, which results in a high resolution in the output signal (resolution offered by DDS-1).

Furthermore, in the phase loop there is no multiplication of the reference frequency, so the level of the phase noise of the output signal in the bandwidth of the PLL is equal to the phase noise of the DDS together with the noise generated by the Phase-Frequency Detector (PFD), by the Charge Pump, and by the Loop Filter. Outside of the bandwidth of the PLL, the phase noise is generated by Voltage Controlled Oscillator (VCO). Depending on a system oscillator (F_C), DDS-1 can provide a relatively small level of phase noise, and a low level of the phase noise of the output signal of the PLL can be achieved by careful selection of the phase loop components. The phase noise at the output of the synthesizer will be less for $20*log(F_S/F_0)$ in comparison with the phase noise of the output signal of PLL.

The phase loop parameters - natural frequency ω_n and damping factor ξ, for the second order unit phase loop and passive filter, are determined using the expressions [9]:

$$\omega_n = \sqrt{\frac{K_0 I_p}{2\pi C}}, \quad \xi = \frac{RC}{2}\sqrt{\frac{K_0 I_p}{2\pi C}} \tag{2}$$

where K_0 (*radians/second/volt*) is the slope of VCO and $I_p(A)$ is current of the Charge pump. Because of the relatively high reference frequency, it is possible to achieve larger ω_n which provides a higher bandwidth of phase loop that is less lock time. The phase looplock time is defined as:

$$Ts = - ln ((f_e/\Delta f) (1-\xi^2)^{1/2})/(\omega_n \xi), \tag{3}$$

where f_e is an acceptable frequency error, Δf is initial frequency error or initial offset [10]. By pre-voltage V_P a small initial offset ($\Delta f = F_{VCO} - F_R$) can be achieved, after which the PLL with high ω_n will quickly reduce the frequency error to an acceptable level f_e. For example, for Δf = 100 KHz, f_e = 100 Hz, ξ = 0,707 and ω_n = 500 KHz the lock time is T_s = 2.23 μs. By selecting a new frequency, the corresponding value of the V_P pre-voltage variation is read from the memory so that the VCO is almost instantly placed very close to the desired frequency. The remaining phase difference is very quickly eliminated by the phase loop. In this way, we get a quick change in the output frequencies, which is especially important in FH-SS systems [11].

III. Results of Measurements

In order to illustrate the possibility of the hybrid synthesizer configuration given in Fig. 2, the chips DDSAD9954 and PLLADF4002 were used. The VCO is realized in the VHF band (60-90 MHz), while the frequencies in the HF band are generated using DDS-2, as an integer part of the output frequency of the PLL.

In Fig. 3, the spectrum of the signal of frequency F_0 = 5.5 MHz is given, in the cases where the system frequency, F_S, for DDS-2 is not an integer multiplier of the output frequency, (F_S/F_0 = 13.6363), as well as F_S is the integermultiplier of the output frequency (F_S/F_0 = 14). In the first case (Fig. 3*a*), the in the output signal arepresent discrete spectral components due to phase shortening. On the other hand, in the case of integer ratio F_S/F_0 (Fig. 3*b*), these spectral components are completely suppressed.

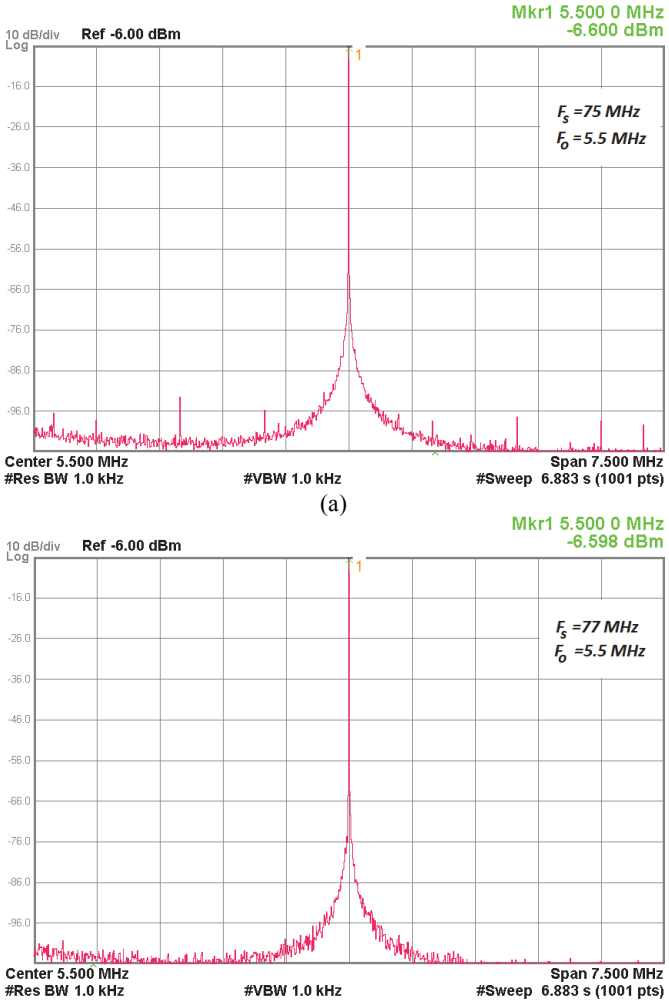
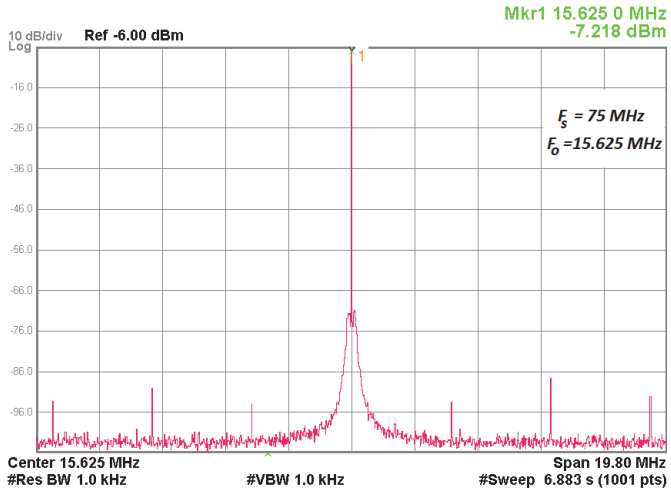


Fig. 3. Spectrum of the signal for: (a) F_S/F_0=13.6363, (b) F_S/F_0=14

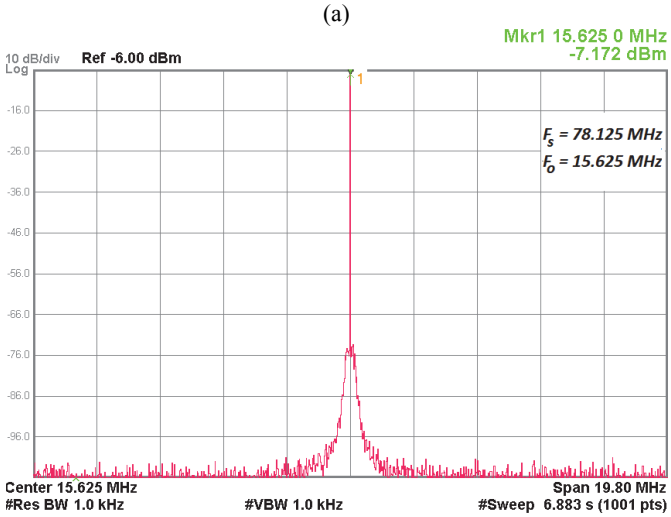
Similarly, Fig. 4 shows the spectrum of the frequency signal F_0 = 15.625 MHz in the cases where the system frequencyand output frequency are in different ratios. In the case where system frequency F_S = 75 MHz (Fig. 4*a*) is not integer multiplier of output frequency (F_S/F_0 = 4.8), the spectral components arepresent due to phase shortening. The spectrum of the same signal, for F_S = 78.125 MHz, where the ratio of frequencies is integer (F_S/F_0 = 5) illustrate the complete suppression of these spectral components (Fig. 4*b*).

As we said, the output and input frequencies are not uniquely related meaning that we can generate the output frequency for another integer ratio F_S/F_0. Fig. 4*c* shows the spectrum of the frequency signal F_0 = 15.625 MHz, with the system frequency F_S = 62.5 MHz, where the ratio F_S/F_0 = 4.

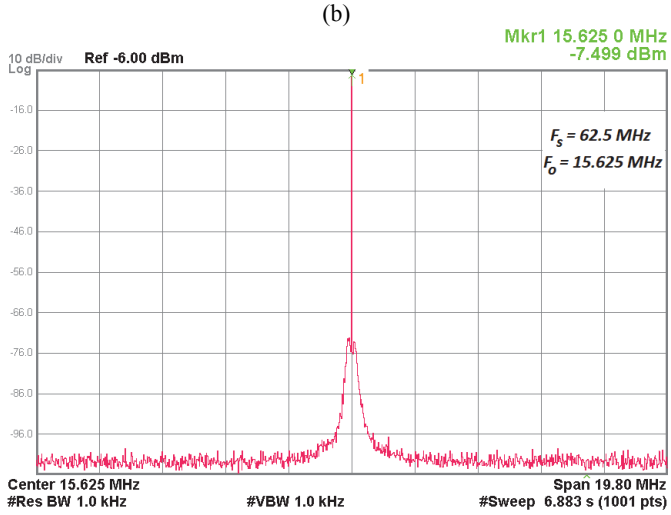
By comparing Figs. 4*b* and 4*c*, a difference in the noise level can be observed. The increased noise level in Fig. 4*c* in relation to Fig. 4*b* is due to a lower frequency of measurement, thereby increasing the spectral power density due to the quantization of the output signal. Therefore, from the available range of frequencies F_S, one should choose the one with the highest integer ratio to the output frequency.



(a)



(b)



(c)

Fig. 4. Spectrum of the signal for:
(a) $F_S/F_0 = 4.8$; (b) $F_S/F_0 = 5$; (c) $F_S/F_0 = 4$.

Finally, Fig. 5 shows the lock time of phase loop. For the specified parametersinitial frequency error Δf = 100 KHz and the loop parameters: ω_n = 200 KHz, $\xi \approx 0.7$, the lock time is within 10 μs, while the calculated value for the allowed error f_e = 100 Hz is T_s = 8.165 μs. Practically, pre-voltage V_P in the VHF band can reduce error $\Delta f \leq$ 10 KHz, which would allow lock time T_s= 2.23 μs for ω_n = 500 KHz.

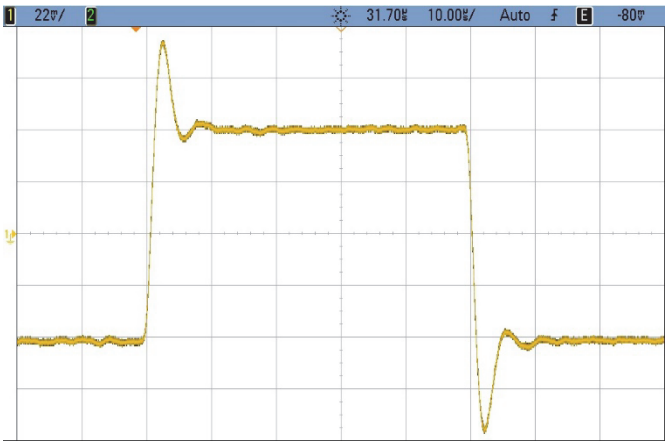


Fig. 5. PLL lock time for Δf = 100 KHz, ω_n = 200 KHz, $\xi \approx 0.7$

IV. Conclusion

In this paper, a solution for generating the FH-SS signal in the HF band is proposed. In that context, the proposal for suppression of spurs due to phase shortening in DDS isverified through the measurement results. The proposed synthesizer has better performances in comparison with signals generated separately by DDS or PLL. A small level of the phase noise of the output signalis achieved, together with short lock time (order of μs), high resolution and spectral purity of the output signal. Also, with the proposed synthesizer the problem of covering more octaves is solved, as well as requirement for voltage-controlled oscillators in the HF band. At the same time, advantages of DDS are retained, such as the possibility of digital modulation, RF signal shaping, output frequency sweep, good suppression of harmonics, etc. Finally, by modifying the proposed scheme it is possible to generate signals in the UHF and microwave bandthat could be the subject of future research.

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