Gain Improvement of the Cascaded Single Stage Distributed Amplifier

Fayçal Amrani[1], Mohamed Trabelsi[2]

Abstract – **In this paper, a high gain cascaded single stage distributed amplifier design method is proposed. This new design method is based on the Chebyshev polynomial approximation of the amplifier transducer gain. By this approximation an improvement of 12 dB in gain, is obtained, compared with the conventional cascaded single stage distributed amplifier with a simplified unilateral single field effect transistor model. This 12 dB are obtained by eliminating two resistors which consume the power; but, by doing this, a mismatch is provoked in the circuit, so a loss of gain is obtained at high frequencies. By the use of the proposed method a stable gain is obtained from dc to the cut-off frequency of the circuit. In addition, a more compact circuit is obtained, by eliminating four components, compared with the cascaded single stage distributed amplifier.**

Keywords – **Distributed amplifiers, bandwidth, cascode, Chebyshev polynomial, cascaded single stage, gain, ripple ratio.**

I. INTRODUCTION

Distributed Amplifiers (DAs) are one of the key components that are employed in electronic warfare, radar, high-data-rate fiber-optic communication, and broadband instrumentation systems. Their structure, formed by active devices coupled with transmission lines, exhibits a broadband characteristic in terms of high gain and bandwidth. To improve these two characteristics, many methods have been reported [1-6].

The Cascaded Single Stage Distributed Amplifier (CSSDA), consisting of a number of cascaded stages, was proposed by J.Y. Liang and C.S. Aitchison [7] (Fig. 1). It is a circuit composed by n unilateral field effect transistor amplifiers (Fig. 2), linked to each other, by artificial transmission lines, according to the cascade topology, these lines are called the inter-stage lines. Each of these inter-stage lines consists of two inductances L and $L_{int}/2$ and the two capacitors gate-source C_{gs} and drain-source C_{ds} of the transistor (Fig. 2). The input line, connecting the generator to the CSSDA first stage, consists of the first transistor capacitance C_{gs} and two inductances $L_{in}/2$ terminated with an impedance Z_0, while the last transistor capacitance C_{ds}, constitute with two other inductances $L_{out}/2$ the output line coupling the CSSDA last stage to the load.

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Therefore, the cut-off frequency and the characteristic impedances of the amplifier depend on the capacitances and inductances of the artificial lines, which are made up of k-constant cells transmitting the signal from dc to the cut-off frequency.

To have a matched circuit, the input, output and the inter-stage lines are terminated respectively by their characteristic impedances Z_o and Z_{oint}. So, a progressive wave propagates all aver the circuit. Therefore, the voltage along the lines remains constant even when the frequency varies from dc to the line cut-off frequency. Thus, a constant current I_{ds} is generated at the output of each transistor, as it is proportional to this voltage $I_{ds} = g_m V_{gs}$ (g_m : the transistor transconductance) (Fig. 2). This will result in a stable available power gain from dc to the artificial transmission lines cut-off frequency, which gives the CSSDA a low pass character.

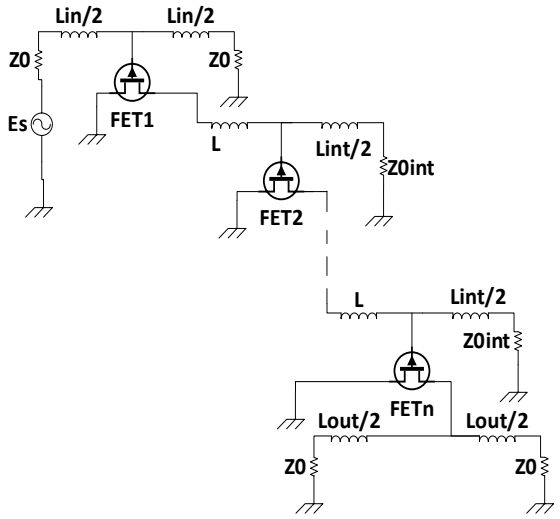

Fig. 1. The CSSDA amplifier

In this paper, another CSSDA, named the Mismatched Cascaded Single Stage Distributed Amplifier (MCSSDA) (Fig. 3), is proposed. In this amplifier, a mismatch is imposed to the input and the output of the circuit, this mismatch is caused by letting the input and output lines opened. Thus, the first transistor voltage V_{gs} and, consequently, the current in the load will be doubled. So, an improvement of 12 dB in gain is provided, in low frequencies, with this new structure. But, because of the input and output lines mismatch, a gain instability can be generated when the frequency changes, and, consequently, a bandwidth which may be relatively narrower. The goal of this work, is to find a solution to these two

disadvantages, and keep a high and stable gain of the amplifier over a large range of frequency.

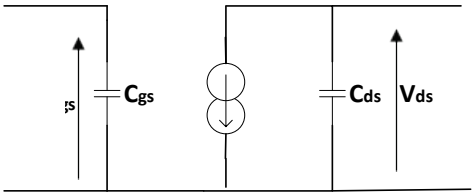

Fig. 2. The simplified unilateral MESFET

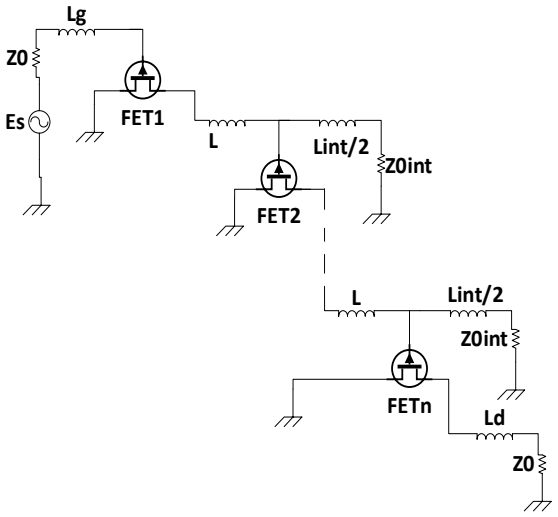

Fig. 3. The MCSSDA amplifier

II. CIRCUIT PRINCIPLE

The transducer power gain of an *n* stages CSSDA amplifier, at low frequency, is given by [7]:

$$G_{T(CSSDA)} = \frac{Z_0^2 Z_{0int}^{2(n-1)} {g_m}^{2n}}{4} \quad (1)$$

The MCSSDA equivalent circuit is given in Fig. 4, where the MESFET transistor is represented by its simplified unilateral model (Fig. 2).

In this circuit, C_{gsi} ($i \in [1, n]$) is the transistor grid-source capacitance, and C_{dsi} ($i \in [1, n\text{-}1]$) is the drain-source capacitance. with $Z_{0int} = \sqrt{\frac{L_{int}}{C_{gs}}}$ the characteristic impedance of the inter-stage lines. To the last capacitance C_{dsn}, we add a shunt capacitance C_l, to obtain $C_d = C_{dsn} + C_l$, that the value will be calculated in the following demonstration.

The MCSSDA gain calculations, based on the equivalent circuit of Fig. 4, gives the following result:

$$G_{T(MCSSDA)} = \frac{4Z_0^2 g_m^{2N} Z_{0int}^{2(N-1)}}{[(1-4x^2)^2 + \alpha_1^2 x^2][(1-4a^2x^2)^2 + \alpha_2^2 a^2 x^2]} \quad (2)$$

where $x = \frac{\omega}{\omega_{c1}}$ is the normalized frequency with respect to the cut-off frequency of the first stage grid line; $\omega_{c1} = \frac{2}{2\pi\sqrt{L_g C_{gs1}}}$, $\alpha_1 = 2\frac{Z_0}{Z_{c1}}$, $\alpha_2 = 2\frac{Z_0}{Z_{cn}}$, and $a = \frac{f_{c1}}{f_{cn}}$ with $Z_{c1} = \sqrt{\frac{L_g}{C_{gs1}}}$ and $Z_{cn} = \sqrt{\frac{L_d}{C_d}}$, the characteristic impedances, at relatively low frequencies, of the k-constant circuits constituting the input grid and the output drain lines respectively, and $f_{cn} = \frac{2}{2\pi\sqrt{L_d C_d}}$ the cut-off frequency of the drain line at the circuit output.

At the DC signal, the CSSDA power transducer gain is $\frac{Z_0^2 Z_{0int}^{2(n-1)} {g_m}^{2n}}{4}$, and that of the MCSSDA is $4Z_0^2 g_m^{2N} Z_{0int}^{2(N-1)}$; this shows an improvement of 12 dB in the MCSSDA gain compared to the CSSDA.

However, since the MCSSDA amplifier input and output are mismatched, the input and output lines will be traversed by stationary waves, which generates ripples in the curve of the MCSSDA gain when the frequency varies.

The main idea of this work, is to keep a constant gain $G_{T(MCSSDA)}$ over the entire frequency band; to achieve this, the denominator of Eq. (2) will be approximated by a polynomial providing low ripple.

In Eq. (2), the term $4Z_0^2 g_m^{2N} Z_{0int}^{2(N-1)}$ is a constant term, so we can normalise $G_{T(MCSSDA)}$ as follows:

$$g_{T(MCSSDA)} = \frac{G_{T(MCSSDA)}}{4Z_0^2 g_m^{2N} Z_{0int}^{2(N-1)}} = \frac{1}{[(1-4x^2)^2 + \alpha_1^2 x^2][(1-4a^2x^2)^2 + \alpha_2^2 a^2 x^2]} \quad (3)$$

As this expression is dimensionless, it can be applied to any field effect transistor and to any line; this fact constitutes an important advantage. The approximation can be done, in that manner:

By developing Eq. (3) the normalized gain $g_{T(MCSSDA)}$ can be rewritten as:

$$g_{T(MCSSDA)} = \frac{1}{(1 + A_2x^2 + A_4x^4 + A_6x^6 + A_8x^8)} \quad (4)$$

where:

$$\begin{cases} A_2 = a^2(\alpha_2^2 - 8) + (\alpha_1^2 - 8) \\ A_4 = 16a^4 + a^2(\alpha_1^2 - 8)(\alpha_2^2 - 8) + 16 \\ A_6 = 16a^4(\alpha_1^2 - 8) + 16a^2(\alpha_2^2 - 8) \\ A_8 = (16)^2 a^4 \end{cases}$$

The Chebyshev polynomial approximation will be made on the $g_{T(MCSSDA)}$ denominator, which will be written in the $D = 1 + Q_n(x)$ form, or:

$$D = (1 - \varepsilon'^2)\left[1 + \varepsilon^2\left(1 + \frac{Q_n(x)}{\varepsilon'^2}\right)\right] \quad (5)$$

where $\varepsilon^2 = \frac{\varepsilon'^2}{1-\varepsilon'^2}$ represents the ripple ratio.

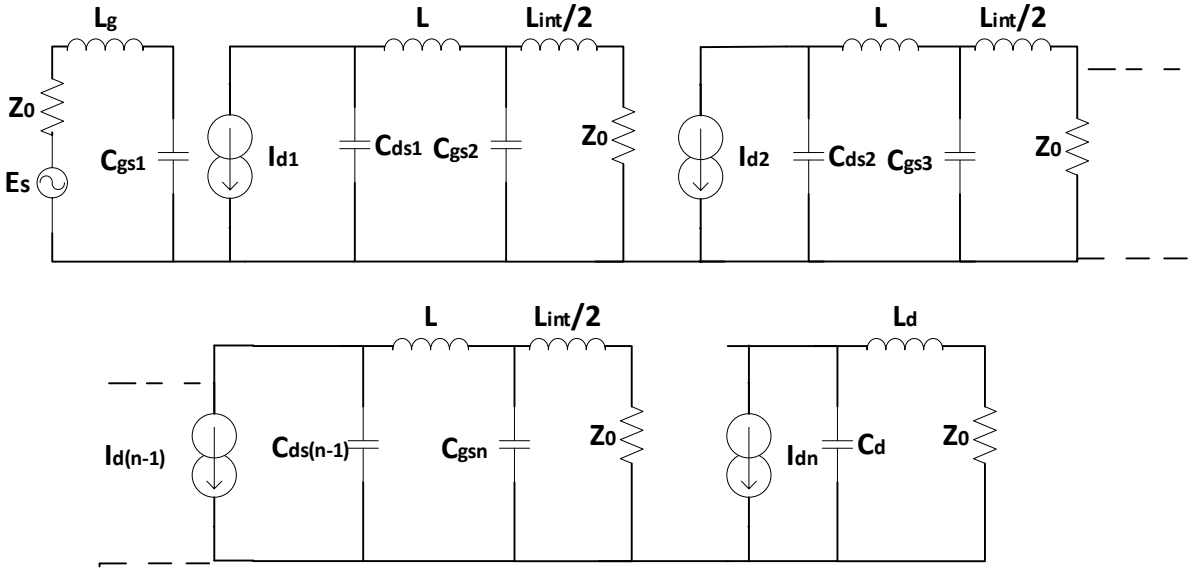

Fig. 4. Equivalent circuit of the MCSSDA

We proceed then to the approximation by the Chebyshev polynomial $T_n^2(x)$ of a part of the denominator D, namely:

$$1+\varepsilon^2\left(1+\frac{Q_n(x)}{\varepsilon'^2}\right)=1+\varepsilon^2 T_n^2(x) \quad (6)$$

Then:

$$T_n^2(x)=1+\frac{Q_n(x)}{\varepsilon'^2} \quad (7)$$

Since $Q_n(x)$ is of degree 8, $T_n^2(x)$ must be of the same degree [8]:

$$T_n^2(x)=64x^8-128x^6+80x^4-16x^2+1 \quad (8)$$

By identifying the Eqs. (4) and (8), we obtain the following system:

$$\begin{cases} A_8=64\varepsilon'^2 \\ A_6=-128\varepsilon'^2 \\ A_4=80\varepsilon'^2 \\ A_2=-16\varepsilon'^2 \end{cases} \quad (9)$$

So, to design the MCSSDA amplifier we must first solve the system of Eq. (9) whose roots are α_1, α_2, a and ε'. The values that these roots are the same whatever the used field effect transistor characteristics are.

The resolution of the system (9) gives the following result:

$$\alpha_1=2.38;\ \alpha_2=0.556; a=0.509;\ \varepsilon^2=0.37 \quad (10)$$

With the values of Eq. (10) and by taking $Z_0=50\ \Omega$, the design parameters as a function of the gate capacitance C_{gs1} may be deduced as:

$$C_{dn}=0.119C_{gs1};\ L_g=1764C_{gs1};\ L_d=3846C_{gs1} \quad (11)$$

The results given by Eqs. (10) and (11) are general and thus they can be applied to any field effect transistor. So, it is sufficient only to know the value C_{gs1} of the used transistor parameter, to proceed to the amplifier design.

We can deduct from the obtained results that the field effect transistors with a ratio $\frac{C_{ds}}{C_{gs}}$ less than 0.119 requires an addition of a shunt capacitor C_l to the drain of the last transistor. The added capacitor forms in combination with C_{dsn} a new capacitor C_d such that $\frac{C_d}{C_{gs1}}=0.119$. The shunt capacitor at the gate should be avoided since it leads to a reduction of the bandwidth.

The graph of the normalized gain $g_{T(MCSSDA)}$ (dB) as a function of the normalized frequency x is given in Fig. 5 where the maximum ripple is 0.37.

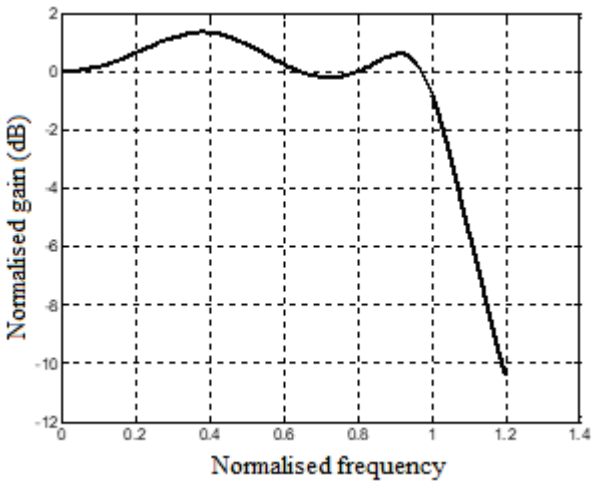

Fig. 5. Normalized gain $g_{T(MCSSDA)}$ (dB) versus normalized frequency

III. Design and Simulation

To validate our method, we must naturally confront the results obtained with those given by the software simulator Advanced Design System. Moreover, through this confrontation, we must highlight the gain improvement that the MCSSDA offers compared to the CSSDA [7]. To accomplish this, the two amplifiers CSSDA and MCSSDA will be designed using a simplified unilateral MESFET transistor having $C_{gs} = 0.17$ pF, $C_{ds} = 0.006$ pF and $g_m = 0.32$ mS as parameters.

Concerning the CSSDA, in order to have characteristic impedance of the input, output and the inter-stage lines $Z_0 = Z_{0int} = 50\ \Omega$. The inductances to be added are calculated using the formula $Z_0 = \sqrt{L/C}$.

For the MCSSDA, the inter-stage lines have an impedance of 50 Ω, so the inductances to be added have the same values as those of the CSSDA, while the input and the output parameters are, after calculation using the Eq. (11), $L_g = 300$ pH and $L_d = 653.2$ pH, and a shunt capacitor of $C_l = 0.014$ pF must be added to the drain of the n^{th} transistor to have $C_{dn} = 0.119C_{gs1}$.

As the characteristic impedances, of the CSSDA artificial lines and the MCSSDA inter-stage lines, are frequency-dependent. A problem of mismatch will then arise at the output of such lines if they are loaded by a resistor of constant value $Z_0 = Z_{0int} = 50\ \Omega$. To overcome this problem, an "m-derived" circuit is interposed between these lines and the load in order to ensure the matching condition [9].

The gains simulation results of the two amplifiers CSSDA and MCSSDA, using a simplified unilateral transistor model, are represented by Fig. 6. This figure shows that the MCSSDA offers an improvement of 12 dB in gain compared to that of the CSSDA.

In addition to the advantage of having an increase of 12 dB in gain, we also have the advantage of maintaining a wide bandwidth despite the input and output lines mismatch. The latter advantage comes from the idea of imposing, by a suitable polynomial approximation (Chebyshev) to the gain $g_{T(MCSSDA)}$, a stable response from dc to the cut-off frequency of the input and output lines.

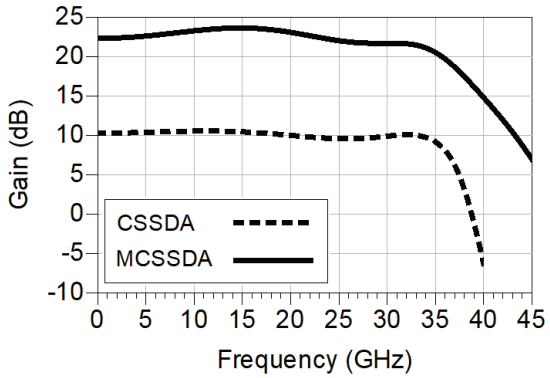

Fig. 6. The gain of four stage CSSDA and MCSSDA amplifiers using a simplified unilateral transistor model

IV. Case where the Transistor is Bilateral

To use our method, the field effect transistor, which we call the simplified transistor (Fig. 2), must be unilateral (transmission coefficient $S_{12} = 0$), and only capacitive at input and output. Moreover, the transconductance g_m must imperatively be constant. However, transistors do not offer all these characteristics as shown in Fig. 7, where the capacitance C_{gd} in particular makes the transistor bilateral. Being bilateral, the transistor, when inserted in the amplifier circuit, will have at its input and output dissipative passive impedances depending on each other, and a variable transconductance, which makes it unusable by our method. So, by using a bilateral transistor in the amplifier design, a deterioration will be obtained in the amplifier performances compared with the amplifier using the simplified unilateral model of the transistor, as shown in Fig. 8. Therefore, in order to make it applicable, we have to find another active device that answers as much as possible to the requirements imposed in this article. The device chosen is the cascode circuit (Fig. 9). This circuit was largely used in distributed amplification in order to improve their performance.

In [10] the authors used the cascode device to improve the power capability of the circuit by having a double polarisation of transistors; to improve the conventional distributed amplifier gain, a capacitive all-pass network is employed on the gate of each cascode cell, the performance obtained is a gain of 16 dB from dc to 20 GHz.

By adding a series capacitance on the gate of the second transistor to fix the power matching between transistor independently of frequency, [11] has optimised the power performance of the cascode cell on bandwidth and could obtain a good performance of the device from 4 to 18 GHz.

Since December 1979 [12], B. J. Hosticka could improve the voltage gain of the CMOS amplifier to be 32000 times of the input, and in 2015 [13] proposed a new method based in a combination of a Hosticka circuit and inductive coupling technique, and could obtain more linearity and less distortion compared with high voltage gain which should be operating in saturation region.

The study [14] showed that, unlike the single-bilateral-transistor circuit, the cascode assembly is practically a unilateral circuit with almost infinite output impedance.

As result, it can be concluded that the circuit which answers the most closely to the requirements imposed by the simplified unilateral transistor is the cascode circuit, so its use remains justified in the distributed amplifiers. In this work an inductor has been added between the two transistors (Fig. 9) in order to reduce, in high frequency, the effect of the output and input capacitances of the first and second transistors. The value of this inductor will be obtained by optimisation using the microwave simulator.

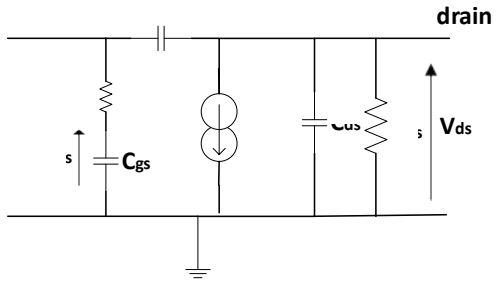

Fig. 7. Equivalent circuit of the field effect transistor

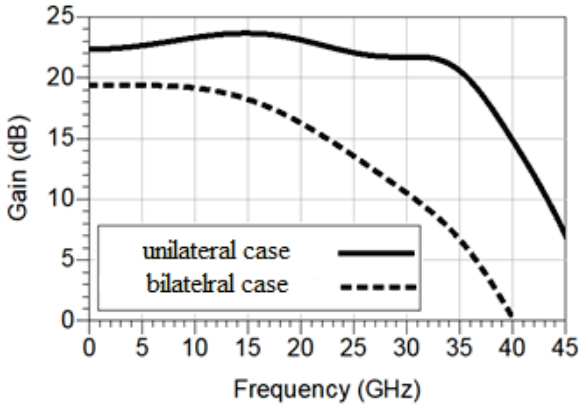

Fig. 8. Gains of the MCSSDA amplifier (unilateral and bilateral cases)

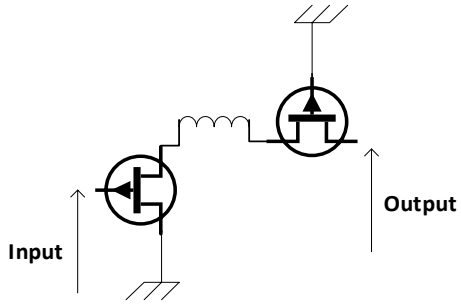

Fig. 9. The cascode circuit

V. Comparison Between Different Designs (Unilateral, Bilateral and Cascode Circuit)

The transistor elements in the bilateral case, Fig. 7, are: $C_{gs} = 0.17$ pF, $C_{ds} = 0.006$ pF, $C_{gd} = 0.016$ pF, $R_{ds} = 560\ \Omega$, $R_{gs} = 0.53\ \Omega$, $g_m = 32$ mS.

In the cascode circuit, the output capacitance is $C_{gd} = 0.016$ pF, so the shunt capacitance which must be added to the last stage is: $C_l = (C_{gs} \times 0.119) - C_{dg} = 0.004$ pF. this capacitance may be neglected in the design as its value is very small.

Fig. 10 shows the simulation results of the three designed amplifiers: CSSDA with bilateral transistor, MCSSDA using bilateral transistor and MCSSDA with cascode circuit. This figure highlights clearly the improvement that our design method brings compared to the conventional technique.

These improvements are given as follows:

• The MCSSDA with cascode offers a higher bandwidth of 6 GHz compared to the CSSDA, which corresponds to an improvement of 25%.

• The MCSSDA with cascode offers a gain improvement of 12.7 dB compared to the CSSDA.

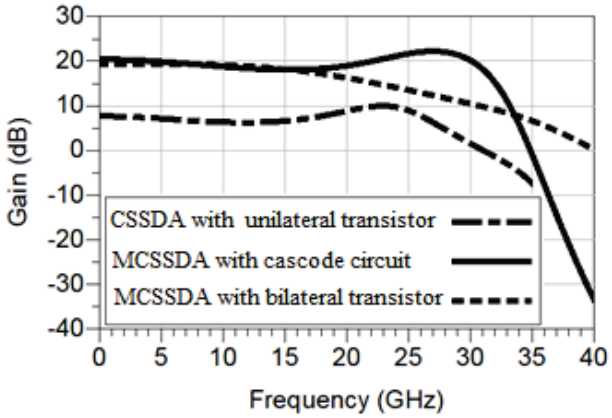

Fig. 10. Gains of the different amplifiers studied

VI. Conclusion

The advantage of the proposed amplifier is the gain improvement of 12 dB compared to that of the CSSDA amplifier using the simplified unilateral model of the field effect transistor or the cascode circuit. Although the input and output lines are mismatched, the bandwidth of the MCSSDA remains equal to that of the CSSDA whose lines are matched. In addition, the MCSSDA uses less input and output components, two resistors and two inductors are eliminated. We can also see that, the cascode mounting improves the bandwidth by 20% compared to the single transistor circuit, this is due to the reduction of the Miller effect. In addition, the gain of the proposed amplifier can be controlled by the inter-stage lines impedance.

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